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3922 63986

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Rev. 8/27/01

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Date 4/8 Serial # 091752,847 Priority Application Date 9/11/00
 Your Name M. Lewis Examiner # _____
 AU 2802 Phone 305-3743 Robin Flara3-3807
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Claims 1-8
Problem see Pg 1 Para 3rd para 4th + 5th
 " 3 " " "
 " 4 " "
Solution " " " 3rd "
 " " 5 1st "

Searcher: <u>LB1114-0814</u>	Type of Search	Vendors
Searcher Phone: <u>306-0435</u>	Bibliographic <input checked="" type="checkbox"/>	_____
Searcher Location: <u>STIC-EIC2800, CP4-9C18</u>	Litigation _____	Quest/Orbit _____
Date Searcher Picked Up: <u>4/16/02</u>	Fulltext _____	Lexis-Nexis _____
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Searcher Prep/Rev Time: <u>90</u>	Other _____	Other _____
Online Time: <u>90</u>		

04/10/2002

Serial No.:09/852,847

FILE 'INSPEC, HCAPLUS' ENTERED

L1 1107371 S (TRENCH## OR HOLE OR GROOVE OR CHANNEL OR EDGE OR FLUSH OR RI
L2 17178 S (SOLDER OR SOLDERING OR SOLDERED OR BRAZ? OR POLYMER?) (2N) (BA
L3 929359 S IC OR ICS OR ((INTEGRATED OR LOGIC) (W) (CIRCUIT)) OR (MICRO) (W
L4 3283181 S CONNECT? OR JOIN### OR COMBINE OR CONJOIN? OR CONJUGAT? OR CO
L5 2630959 S WIR### OR LIN###
L6 284761 S STACK### OR MOUNT? OR PILE OR PILED OR MOUND?
L7 3649 S L3 AND L2
L8 847 S L7 AND L5
L9 136 S L8 AND RESIN
L10 33 S L9 AND L1
L11 33 DUP REMOVE L10 (0 DUPLICATES REMOVED)
L12 290 S L8 AND L6
L13 186 S L12 AND L4
L14 14353 S (ELECTRICALLY) (2N) (CONNECT? OR JOIN? OR INTERCONNECT)
L15 25 S L13 AND L14
L16 25 DUP REMOVE L15 (0 DUPLICATES REMOVED)
L17 21 S L16 NOT L11
L18 22 S L9 AND L14
L19 6 S L18 NOT (L11 OR L17)
L20 1704 S L7 AND L4
L21 467 S L20 AND L5
L22 186 S L21 AND L6
L23 36 S L22 AND RESIN
L24 15 S L23 NOT (L10 OR L15 OR L18 OR L19)

FILE 'WPIX, JAPIO'

L25 16017 S L7
L26 9395 S L25 AND L4
L27 1601 S L25 AND L14
L28 3625 S L26 AND L5
L29 982 S L28 AND L1
L30 446 S L29 AND L6
L31 792 S L27 AND L5
L32 398 S L31 AND L6
L33 127 S L32 AND L1
L34 62 S L33 AND ELECTRODE

L34 ANSWER 1 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
 AN 2001-528966 [58] WPIX
 CR 2001-410362 [44]
 DNN N2001-392574 DNC C2001-157706
 TI Flexible **wiring** board for use in liquid crystal display devices, comprises thin polymer film which is rendered freely bendable in the vicinity of semiconductor **chip mounting** region.
 DC A85 L03 U11
 IN SAITO, H
 PA (CASK) CASIO COMPUTER CO LTD; (CASK) CASIO MICRONICS KK; (SAIT-I) SAITO H
 CYC 4
 PI US 2001009299 A1 20010726 (200158)* 21p
 JP 2001210676 A 20010803 (200159) 6p
 JP 2001284751 A 20011012 (200176) 10p
 CN 1316871 A 20011010 (200207)
 KR 2001078040 A 20010820 (200212)
 ADT US 2001009299 A1 US 2001-766269 20010119; JP 2001210676 A JP 2000-16492 20000126; JP 2001284751 A JP 2000-372946 20001207; CN 1316871 A CN 2001-102313 20010131; KR 2001078040 A KR 2001-3501 20010122
 PRAI JP 2000-372946 20001207; JP 2000-16491 20000126; JP 2000-16492 20000126
 AB US2001009299 A UPAB: 20020130
 NOVELTY - A flexible **wiring** board comprises a thin polymer film which is rendered freely bendable in the vicinity of a semiconductor **chip mounting** region.
 DETAILED DESCRIPTION - A flexible **wiring** board for connection to an electronic part comprises:
 (a) a film (47);
 (b) connection terminals (45a, 45b) electrically arranged in the connection terminal region of the film; and
 (c) drawing wirings (45c) which **electrically connect** the **connection** terminals and the semiconductor **chip** (43).
 The film has a semiconductor **chip mounting** region, a connection terminal region, and an inclined **wiring** region, which is to be bent freely and positioned between the connection terminal region and the semiconductor **chip mounting** region. The drawing **wiring** has an inclined **wiring** section that is to be bent freely, and arranged in the inclined **wiring** region of the film.
 INDEPENDENT CLAIMS are also included for:
 (A) a display device comprising (i) the flexible **wiring** board and (ii) a display panel (31) **electrically connected** to the connection terminals of the flexible **wiring** board; and
 (B) a method of manufacturing a flexible **wiring** board connected to a semiconductor **chip**, comprising:
 (i) heating one surface of the semiconductor **chip**,
 (ii) aligning metallic-made **bump electrodes** arranged on the opposite surface of the semiconductor **chip** with the connection terminals formed on one surface of the flexible **wiring** board, and
 (iii) applying a pressure while heating an opposite surface of the flexible **wiring** board to bond the **bump electrodes** to the connection terminals.
 USE - In electronic parts, e.g. liquid crystal display devices.
 ADVANTAGE - Since the connection terminals are formed to include inclined regions positioned to be gradually apart from the semiconductor

chip together with the film substrate from the portions bonded to the bump electrodes toward the outside of the mounting region of the semiconductor chip, it is possible to prevent the number of manufacturing steps from being increased. Since a bonding tool is brought into direct contact with the other surface of the film substrate under certain conditions with the semiconductor chip kept heated so as to pressurize the semiconductor chip under heat, a bonding of high reliability is obtained, even where the film substrate has one surface corresponding to one surface of the semiconductor chip over the entire mounting region of the semiconductor chip and other surfaces. Since a device hole is not formed in the semiconductor chip mounting region of the film substrate, it is possible to prevent the connection terminals mounted to the film substrate from being deformed. The flexible wiring board can be bent easily in the vicinity of a semiconductor chip mounting region without forming slits for facilitating the bending in the film substrate, thus it is possible to decrease the length of that portion of the flexible wiring board that is positioned ahead of the semiconductor chip mounting region. It can also be miniaturized while maintaining a good connection and can be made excellent in the mounting capability with a high mounting density. Manufacturing cost can be lowered.

DESCRIPTION OF DRAWING(S) - The figure shows a view of a liquid crystal display module mounted to a circuit board.

Display panel 31

Semiconductor chip 43

Connection terminals 45a, 45b

Drawing wirings 45c

Film 47

Dwg.4/14

L34 ANSWER 2 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2001-238336 [25] WPIX

DNN N2001-170515 DNC C2001-071877

TI Flip-chip mounted semiconductor device with external electrode connected to electrode of semiconductor on baseboard, and underfill resin (whose viscosity decreases at specified temperature lower than curing temperature).

DC A85 L03 U11

PA (NIDE) NEC CORP

CYC 1

PI JP 2001024029 A 20010126 (200125)* 8p

ADT JP 2001024029 A JP 1999-191068 19990705

PRAI JP 1999-191068 19990705

AB JP2001024029 A UPAB: 20010508

NOVELTY - Flip-chip mounted semiconductor device has a semiconductor chip with a bump on an external terminal; a base board which has an electrode at a position in alignment with the bump, where the electrode and the external terminal are connected through the bump; and underfill resin filling the space between the semiconductor chip and the base board. The underfill resin is one whose viscosity reduces when heated to at least 200 deg. C, and which starts to harden when heated to 220 deg. C or more.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for the manufacture of a flip-chip mounted semiconductor device, by a process which arranges an underfill resin sheet (where a hole is formed of a size which receives the bump of a semiconductor chip) between a semiconductor chip which

has several bumps on an external terminal, and a semiconductor base board where an **electrode** is provided aligned with the bumps. The sheet is place so that the bump is received in the **hole**, and the bump is reflow-processed.

=> D BIB AB L34 3-62

L34 ANSWER 3 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2001-154180 [16] WPIX

DNN N2001-113752

TI Multichip semiconductor module for use in information providing terminal, has packing resin that is filled between semiconductor **chips**, so that it does not fill into concave **groove** formed on **wiring** board.

DC U11

PA (HITA) HITACHI LTD

CYC 1

PI JP 2000357768 A 20001226 (200116)* 9p

ADT JP 2000357768 A JP 1999-170688 19990617

PRAI JP 1999-170688 19990617

AB JP2000357768 A UPAB: 20010323

NOVELTY - Several semiconductor **chips** (1) are **electrically connected** to the **wiring** board (3), via **bump electrode**. A liquid resin layer (7) is filled in the gap between the semiconductor **chip** and **wiring** board. The packing resin is filled inbetween semiconductor **chips** such that it does not fill into the concave **groove** (10) formed on **wiring** board.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for multichip semiconductor module manufacturing method.

USE - Multichip semiconductor module for use in information providing terminal.

ADVANTAGE - As **mounting** space of semiconductor **chip** is narrowed, the size of semiconductor device is reduced. Avoids disconnection of semiconductor **chips**, thereby reliability is improved.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic diagram of the multichip semiconductor module.

Semiconductor **chips** 1

Wiring board 3

Liquid resin layer 7

Concave **groove** 10

Dwg.1/12

L34 ANSWER 4 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2000-434803 [38] WPIX

DNN N2000-324843

TI **Electrodes** connecting mechanism in semiconductor device, has low melting solder which melts during **mounting**, such that surface and **connection electrodes** are **electrically connected**.

DC U11

PA (HITA) HITACHI LTD; (HITA-N) HITACHI YONEZAWA DENSHI KK

CYC 1

PI JP 2000150732 A 20000530 (200038)* 9p

ADT JP 2000150732 A JP 1998-315257 19981106

PRAI JP 1998-315257 19981106

AB JP2000150732 A UPAB: 20000811

NOVELTY - An insulating sheet (2) has through-holes (2a)

corresponding to surface **electrode** (1a) of semiconductor **chip** (1). A low melting solder (3) functioning as external terminal, melts during **mounting** to **mounting** substrate (4) and **electrically connects** the surface **electrode** (1a) of **chip** and connection **electrode** (4a) of **mounting** substrate.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device manufacturing method.

USE - In semiconductor device.

ADVANTAGE - Avoids usage of **solder ball** in through-hole. Since low melting solder does not project until it **mounts** a semiconductor device in **mounting** substrate, the solder is prevented from dropping in between or ejects deformed, thus inferior **mounting** of semiconductor device is reduced. Since low melting solder acts as external terminal, solder is regulated by volume of through-hole, hence quantity of solder is enhanced, thereby connection reliability is raised during **mounting**. Since solder is formed, **wire** bonding is eliminated, thus manufacturing process of semiconductor device is simplified. Alleviates contamination of low melting solder, electric shock generation is prevented, thereby improves **mounting** property of semiconductor device.

L34 ANSWER 5 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2000-103040 [09] WPIX

DNN N2000-079758

TI Semiconductor device e.g. ball grid array package.

DC U11 V04

PA (SHIH) SEIKO EPSON CORP

CYC 1

PI JP 11345826 A 19991214 (200009)* 8p

ADT JP 11345826 A JP 1999-94101 19990331

PRAI JP 1998-85990 19980331

AB JP 11345826 A UPAB: 20000218

NOVELTY - The semiconductor device (8) has a semiconductor **chip** (10) **mounted** and **electrically connected** to a **wiring** board (12). A polar zone (14) is distributed by the **wiring** board. **Bump electrodes** (16) for external connection are distributed by the polar zone. A **groove** (20) is formed on each **bump electrode**.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:

(a) the semiconductor device manufacture;

(b) and the **mounting** procedure of the semiconductor device.

USE - None given.

ADVANTAGE - Suppresses generation of void when manufacturing and **mounting** semiconductor device.

DESCRIPTION OF DRAWING(S) - The figure is a sectional view showing the structure of the semiconductor device.

Semiconductor device 8

Semiconductor **chip** 10

Wiring board 12

Polar zone 14

Bump electrodes 16

Groove 20

Dwg.1/7

L34 ANSWER 6 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1999-450245 [38] WPIX

DNN N1999-336726

TI Semiconductor device with ball grid array BGA package - has solder resist that coats **wiring** on main surface of package substrate, and solder resist interposed between solder resist for **wiring** and **die** bond material.

DC U11

PA (HITA) HITACHI LTD

CYC 1

PI JP 11186440 A 19990709 (199938)* 8p

ADT JP 11186440 A JP 1997-352995 19971222

PRAI JP 1997-352995 19971222

AB JP 11186440 A UPAB: 19990922

NOVELTY - The semiconductor device has a solder resist (10) that coats a **wiring** (5) formed on the main surface of a package substrate (1). Another solder resist (11) is interposed between the solder resist (10) and **die** bond material (7a). A semiconductor **chip** (2) is **mounted** on the main surface of the package substrate through the **die** bond material. DETAILED DESCRIPTION - **Bump electrodes** (9) are attached at the bottom of the package substrate, and **electrically connected** to the **wiring** through a **hole** (8) formed at the inside layer of

the package substrate. Bonding **wires** (6) **electrically connect** the semiconductor **chip** and the **wiring**.
Resin (3) seals the semiconductor **chip**.

USE - None given.

ADVANTAGE - Reduces stress caused by thermal expansion coefficient difference between the package substrate and semiconductor **chip** since the two layers of solder resist absorb the generated stress. Prevents disconnection of **wiring** formed on package substrate. Has no increase in number of parts and does not need complicated erector for BGA. DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of the semiconductor device with BGA package. (1) Package substrate; (2) Semiconductor **chip**; (3) Resin; (5) **Wiring**; (6) Bonding **wires**; (7a) Die bond material; (8) **Hole**; (9) **Bump electrodes**; (10,11) Solder resist.
Dwg.2/7

L34 ANSWER 7 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-410585 [35] WPIX
DNN N1999-306947

TI **Wiring** board for flip-**chip** mounting of semiconductor devices such as semiconductor **integrated circuit** packages in various electronic devices - includes via **hole** that is formed near periphery of **mounting** area **mounted** with semiconductor device.

DC U11

PA (KYOC) KYOCERA CORP

CYC 1

PI JP 11163196 A 19990618 (199935)* 6p

ADT JP 11163196 A JP 1997-324973 19971126

PRAI JP 1997-324973 19971126

AB JP 11163196 A UPAB: 19990908

NOVELTY - A **wiring** conductor (3) is formed in the inner side or on an insulated base (1). A semiconductor device with **electrode** is **mounted** in the **mounting** area of the insulated base. In the **mounting** area, a **bump** conductor (7) connects **electrode** of semiconductor device. A via conductor (2) is connected to **wiring** conductor. Via **hole** (5) is formed at periphery of the **mounting** area.

USE - For flip-**chip** mounting of semiconductor device such as semiconductor **integrated circuit** packages in various electronic devices.

ADVANTAGE - Via **hole** is made as same as that of via conductor thereby reduces number of manufacturing processes involved. Semiconductor device can be **mounted** with good reproducibility and with high positional accuracy. The **electrode** and via conductor can be aligned correctly and can be **electrically connected** reliably. DESCRIPTION OF DRAWING(S) - The figure depicts the sectional view of the **wiring** board. (1) Insulated base; (2) Via conductor; (3) **Wiring** conductor; (5) Via **hole**; (7) **Bump** conductor.
Dwg.1/2

L34 ANSWER 8 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-239296 [20] WPIX
DNN N1999-178562 DNC C1999-070245

TI **Chip** mounting structure in semiconductor device - has **chip** surface electric conduction layer and electric conduction shield layer **connected electrically**, using **bump electrode**.

04/10/2002

Serial No.:09/852,847

DC L03 U11
PA (SUME) SUMITOMO ELECTRIC IND CO
CYC 1
PI JP 11068029 A 19990309 (199920)* 8p
ADT JP 11068029 A JP 1997-219537 19970814
PRAI JP 1997-219537 19970814
AB JP 11068029 A UPAB: 19990525

NOVELTY - An electric conduction shield layer (16) is formed in a substrate (2) on which a semiconductor **chip** (6) is **mounted**. The **chip** includes a **chip** surface electric conduction layer (12). The **chip** surface electric conduction layer and the electric conduction shield layer are **connected electrically** using a **bump electrode** (18). DETAILED DESCRIPTION - A current carrying portion (10) connects the **chip** back side electric conduction layer (8) and a **chip** surface electric conduction layer (12) via connection **hole**. A through-hole (26) **electrically connects** the substrate back side electric conduction layer (24) and the electric conduction shield layer (16).

USE - In semiconductor device.

ADVANTAGE - Cuts off the external noise from the surface by **electrically connecting** the conductive layers.

DESCRIPTION OF DRAWING(S) - The figure shows sectional view of cross-section line of semiconductor device. (2) Substrate; (6) Semiconductor **chip**; (8) **Chip** back side electric conduction layer; (10) Current carrying portion; (12) **Chip** surface electric conduction layer; (16) Electric conduction shield layer; (18) **Bump electrode**; (24) Substrate back side electric conduction layer; (26) Through-hole current carrying portion.
Dwg.2/7

L34 ANSWER 9 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1999-239110 [20] WPIX
DNN N1999-178376

TI Flip-**chip** connecting structure for package of semiconductor **chip** - includes heat resistant base which performs gold-tin liquid phase reaction **connection** between **electrically** conductive gold bump and tin plated pad at **edge** of **wiring**.

DC U11
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 11067827 A 19990309 (199920)* 7p
ADT JP 11067827 A JP 1997-226674 19970822
PRAI JP 1997-226674 19970822
AB JP 11067827 A UPAB: 19990525

NOVELTY - Several **electrode** pads (8) provided with Au bump (4) are arranged to peripheral of main surface of semiconductor **chip** (2). **Edges** of **wiring** (61) which connect main surface and rear-side electrically, are provided with Sn plated pad (51). Polyimide heat resistant base (11) performs Au-Sn liquid phase reaction connection between pad and bump.

USE - For package of semiconductor **chip**.

ADVANTAGE - Since **chip** is **mounted** on heat resistant base, minute connection is performed by low cost and reduces size of package. Offers package which **mounts** semiconductor **chip** that requires semiconductor **chip** of multi-terminal and high speed operation. DESCRIPTION OF DRAWING(S) - The figure shows cross-sectional view of semiconductor device for flip-**chip**

connection. (2) Semiconductor **chip**; (4) Gold **Bump**; (8) **Electrode** pads; (11) Heat resistant base; (51) Tin plated pad; (61) **Wiring**.
Dwg.1/6

L34 ANSWER 10 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1999-196621 [17] WPIX

DNN N1999-144887

TI Multi-**chip** module - has connection location of conductivity block or through **hole** and base substrate, separated by other base substrate and insulating film from other section of base substrate comprising island-like **electrode**.

DC U11

PA (HITA) HITACHI LTD

CYC 1

PI JP 11040740 A 19990212 (199917)* 4p

ADT JP 11040740 A JP 1997-189468 19970715

PRAI JP 1997-189468 19970715

AB JP 11040740 A UPAB: 19990503

NOVELTY - The connection location of a conductivity block or through **hole** and a base substrate (1) is separated by other base substrate and an insulating film from other section of the base substrate comprising an island-like **electrode**. DETAILED DESCRIPTION - A base substrate with a flat surface consisting of a metal and a semiconductor material, is provided with a metallic earthing conducting layer. A bare-**chip** component having a metallic **bump** (4) on the **electrode** is mounted in the base substrate. The first insulating film (5) of resin shape is covered so that the bare-**chip** component can be embedded. The insulating film and the bump on a bare **chip** (3) are made flat at the same predetermined height. A multilayer interconnection pattern is formed in a metal layer and the insulating film. The bump and part of the multilayer interconnection pattern are **electrically connected**. INDEPENDENT CLAIM is also included for the manufacturing method for a multi-**chip** module.

USE - None given.

ADVANTAGE - Improves predetermined characteristic in high-frequency area since lead **wire** can be shortened when **mounting** the multi-**chip** module in a mother board. Provides strong electromagnetic shielding effect for predetermined interference.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of a multi-**chip** module. (1) Base substrate; (3) Bare **chip**; (4) Metallic bump; (5) First insulating film.

Dwg.1/5

L34 ANSWER 11 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1998-527258 [45] WPIX

DNN N1998-412291

TI Semiconductor device **mounting** structure for printed **wiring** board - involves connecting bump of **chip** to respective **electrode**, **electrode** of substrate to respective **electrode**, and **electrodes** of **chip** and substrate side connectors, by thermocompression bonding.

DC U11 V04

PA (RICO) RICOH KK

CYC 1

PI JP 10233414 A 19980902 (199845)* 5p

ADT JP 10233414 A JP 1997-52351 19970219

PRAI JP 1997-52351 19970219

AB JP 10233414 A UPAB: 19981118

The structure includes **chip** and substrate side connectors (10,12) arranged between a **chip** (2) and a **mounting** substrate (6). The **chip** and substrate side connectors are made of glass epoxy and ceramic aluminium, respectively. A pair of **chip electrodes** (14,16) are formed in the front and rear surfaces of the **chip** side connector. The **chip electrodes** are connected through an **electrically** conductive material embedded in a through hole.

A pair of substrate **electrodes** (20,18) are provided in the substrate side connector, and connected through **electrically** material embedded in respective through hole. A bump (4) of the **chip** is connected to the **chip** side **electrode** (14), by thermocompression bonding. The connection between an **electrode** (8) provided in the substrate and **electrode** (18) provided in substrate side connector, and between **electrodes** (16,20) of **chip** and substrate side connectors is also performed by thermocompression bonding.

ADVANTAGE - Reduces stress due to difference in thermal expansion coefficients of **chip** and substrate.

Dwg.1/4

L34 ANSWER 12 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1998-226811 [20] WPIX

DNN N1998-180295

TI Socket for **mounting** BGAIC on test substrate - has contact pin with lower end that is **electrically** connected to test substrate, and upper end **electrically** connected to solder bump of tested IC.

DC S01 U11 V04

IN FUKAYA, F; HASEYAMA, M; MARUYAMA, S; MIZUKOSHI, M

PA (FUJIT) FUJITSU LTD

CYC 2

PI JP 10069955 A 19980310 (199820)* 24p

US 6229320 B1 20010508 (200128)

US 2001011898 A1 20010809 (200147)

ADT JP 10069955 A JP 1996-227185 19960828; US 6229320 B1 CIP of US 1995-531449 19950921, US 1997-820357 19970312; US 2001011898 A1 CIP of US 1995-531449 19950921, Cont of US 1997-820357 19970312, US 2001-809204 20010316

FDT US 6229320 B1 CIP of US 5854558; US 2001011898 A1 CIP of US 5854558, Cont of US 6229320

PRAI JP 1996-227185 19960828; JP 1994-285342 19941118

AB JP 10069955 A UPAB: 20010615

The socket has a contact unit (23) equipped with an elastic member (31) supporting several contact pins (30). The lower end of the contact pin is **electrically** connected to a test substrate (32). The upper end of the **linear** contact pin is connected to a solder bump (28) of a tested IC (25).

The upper end of the **linear** contact pin is inserted into the solder bump for **electrically** connecting the solder bump of the tested IC with the upper end of the contact pin.

ADVANTAGE - Inhibits damage to **bump electrode**. Tests BGAIC precisely. **Mounts** tested IC accurately on test substrate. Simplifies formation of through-hole and connection of **wiring** pattern with through-hole in substrate.

Dwg.3/25

L34 ANSWER 13 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

04/10/2002

Serial No.:09/852,847

AN 1998-101414 [09] WPIX
DNN N1998-081261
TI Low-EMI **circuit** board and low-EMI cable connector - comprises
shield **plate** connected to **electrode** patterns,
electrically connected to ground layer through
holes along periphery of multilayered **circuit** board.
DC V04
IN AKIBA, Y
PA (HITA) HITACHI LTD
CYC 22
PI WO 9802025 A1 19980115 (199809)* JA 55p
RW: AT BE CH DE DK ES FI FR GB GR IE IT LU MC NL PT SE
W: CN KR SG US
JP 10027987 A 19980127 (199814) 18p
EP 914032 A1 19990506 (199922) EN
R: DE FR GB NL
US 6188297 B1 20010213 (200111)
ADT WO 9802025 A1 WO 1997-JP2376 19970709; JP 10027987 A JP 1996-180863
19960710; EP 914032 A1 EP 1997-930733 19970709, WO 1997-JP2376 19970709;
US 6188297 B1 WO 1997-JP2376 19970709, US 1998-202926 19981223
FDT EP 914032 A1 Based on WO 9802025; US 6188297 B1 Based on WO 9802025
PRAI JP 1996-180863 19960710
AB WO 9802025 A UPAB: 19980410
Such **circuit** parts as an LSI element (8) which generates
radiation of a differential mode is **mounted** on the surface of a
multilayered **circuit** board (1) and the entire surface of the
board (1) including the **circuit** parts is covered with a shield
plate (12) carrying a loss layer (14) on the substrate (1) side so as to
efficiently reduce the radiation centred around the differential mode
generated from the parts, etc., **mounted** on the board (1). The
plate (12) is fixed or connected to many **electrode** patterns
(6a,6g,6h,6n, etc.), **electrically connected** to a
ground layer (2) through **holes** (5) along the entire periphery of
the board (1) with solder (7), etc. In this case, connections are made
directly by the ground layer (2) and through **holes** (5), or
through a matching terminating **chip** resistor (10).
A low-EMI cable connector is composed of (n) pieces (n = 1,2,...) of
cylindrical bodies carrying dielectric sections which surround the entire
periphery of a transmission cable on their internal surfaces and a
short-circuiting terminating **line** is formed on the terminating
end sides of the cylindrical bodies by providing short-circuiting members
which surround the entire circumference of the cable and the resonance
frequency of the **line** is made equal to that of the transmission
cable.
ADVANTAGE - Unnecessary generated radiation is confined in space
between ground layer and plate and, at the same time, converted into Joule
heat. Leakage of unnecessary radiation of common mode from side face of
board is also suppressed.

1

Dwg.1/13

L34 ANSWER 14 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1996-511343 [51] WPIX
DNN N1996-431180 DNC C1996-160125
TI Resin sealed semiconductor device equipped with ball like external
terminal for **mounting** on PCB - has **ball-like**
electrode that is **electrically connected** with
wiring formation surface of PCB with **wire**.
DC A85 L03 U11

PA (SHAF) SHARP KK

CYC 1

PI JP 08264678 A 19961011 (199651)* 5p

ADT JP 08264678 A JP 1995-68124 19950327

PRAI JP 1995-68124 19950327

AB JP 08264678 A UPAB: 19961219

The device consists of a semiconductor **chip** (1) that contains a **circuit** formation surface. A PCB (2) has a **wiring** formation surface whose area is smaller than area of semiconductor **chip**. The **circuit** formation surface and back side of **wiring** formation passage are joined together by an adhesive agent (6). The area surrounding a **ball-like electrode** (4) that is **linked** to a **wire** (5) of **wiring** formation surface, is removed.

A top coat that contains a protective resin (7) such as fluorine system resin is formed. The **wire** connects the **electrode** formed in the periphery of the **chip** and **wiring** formed in the PCB, electrically. A second protective resin (3) of epoxy system is formed in the **wire**.

ADVANTAGE - Reduces formation of poor connections. Realizes size reduction. Enables reuse of semiconductor **chip** in ease if **wiring** defect occurs. Enables reuse of device effectively. Reduces size of device. Prevents impairing of electric connection between **electrode** and PCB. Eliminates need of through **hole**.

Dwg.1/4

L34 ANSWER 15 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1996-430632 [43] WPIX

DNN N1996-362997

TI Multi-**chip** module semiconductor device - has two substrates, one whose opposing surface w.r.t. its **mounting** surface with other substrate is fixed at **bump electrode**.

DC U11

PA (FUIT) FUJITSU LTD

CYC 1

PI JP 08213497 A 19960820 (199643)* 8p

ADT JP 08213497 A JP 1995-17257 19950203

PRAI JP 1995-17257 19950203

AB JP 08213497 A UPAB: 19961025

The device includes a substrate (12) where a **wiring** layer is provided. The substrate has a **chip** case (15) provided with a **hole**. Another substrate (13) is flexibly attached to the substrate (12). A **bump electrode** is provided with a soldering material set as an outer connection terminal. A semiconductor **chip** (11) is **electrically** and mechanically **connected** at the substrate (12) **wiring** layer.

The substrates are electrically and mechanically fixed with each other. The opposing surface of the substrate (13) w.r.t. its **mounting** surface with the substrate (12) is attached at the **bump electrode**.

ADVANTAGE - Ensures easy handling process by having durable pin. Easily checks mfg. process. Achieves inexpensive pin cost.

Dwg.2/7

L34 ANSWER 16 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1996-126112 [13] WPIX

DNN N1996-106222

TI Optimum **integrated circuit** socket for semiconductor device inspection - has substrate for **connection** with

electrically conductive layers arranged to correspond to electrodes of bare chip for inspection with wiring connected to conductive layers.

DC S01 U11
PA (YAWA) NIPPON STEEL CORP
CYC 1
PI JP 08022875 A 19960123 (199613)* 5p
ADT JP 08022875 A JP 1994-175972 19940705
PRAI JP 1994-175972 19940705
AB JP 08022875 A UPAB: 19960405

The socket (1) includes electrically conductive layers arranged in a substrate for connection (6) corresponding to the electrode parts of a semiconductor chip (7) which should be inspected. The substrate for connection is held by a substrate holder (5).

It has metal balls (10) whose arrangement junctions are made on each through hole (8) part of the substrate. Wiring (9) is connected to each metal ball, is provided which comes in contact to the contact (11a) of an external connector terminal (11).

USE/ADVANTAGE - For electric test of semiconductor device mounted in circuit substrate without using lead for external connection. Eliminates reformation of bump or excellent-article chip of solder after test. Enables remarkably simplified process inspection of manufacturing process. Inspects semiconductor chip easily and reliably even on bare chip which has bump in electrode part. Obtains very large applicability on various types of semiconductor chips without bumps in electrode parts.

Dwg.1/8

L34 ANSWER 17 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1995-287025 [38] WPIX
DNC C1995-129110
TI Semiconductor device mfr. applied to ball grid array package - comprises patterning process to prepare land pattern, electrode connection terminal and ball grid array in fixed pattern.
DC L03
IN AHN, S H; KWON, Y S; AHN, S; KWON, Y
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 4
PI JP 07183426 A 19950721 (199538)* 7p
US 5594275 A 19970114 (199709) 8p
CN 1106164 A 19950802 (199730)
KR 9700214 B1 19970106 (199932)
ADT JP 07183426 A JP 1994-285124 19941118; US 5594275 A US 1994-345385
19941118; CN 1106164 A CN 1994-117079 19941005; KR 9700214 B1 KR
1993-24581 19931118
PRAI KR 1993-24581 19931118
AB JP 07183426 A UPAB: 19950927

The semiconductor device is mounted on the main substrate (31). A through hole is formed on both sides of the main substrate through a plating process and copper, nickel and another metals are plated sequentially focusing on a through hole to generate a plating layer (35). A land pattern is prepared by patterning process.

An electrode connection terminal (33) is formed on the main substrate for lead bonding. The ball grid array is formed on the plating layer (35). The semiconductor chip is mounted through the adhesive agent, in the central region of the main substrate. Then wire bonding is performed to electrode connection terminal. The solder balls (36) are fixed on the

plating layer (35).

ADVANTAGE - Increases reliability. Improves mounting efficiency. Provides three dimensional surface mount.
Dwg.1/8

L34 ANSWER 18 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1995-120222 [16] WPIX

DNN N1995-094715 DNC C1995-055336

TI Semiconductor device manufacturing method - involves forming holes by side of transistor with **electrodes** connected and each terminal connection to respective **electrodes** by connectors fusing **bumps**.

DC L03 U11

PA (HITA) HITACHI LTD

CYC 1

PI JP 07045620 A 19950214 (199516)* 9p

ADT JP 07045620 A JP 1993-203616 19930726

PRAI JP 1993-203616 19930726

AB JP 07045620 A UPAB: 19950502

The semiconductor device manufacturing method involves formation of **holes** (23 - 25) by the side of transistor (40). **Electrodes** connected **electrically** to the transistor **circuit** are formed by the circumferential side of each **hole**.

Bumps are formed on each **electrode**. Each **bump** is fused by the collector terminal(53), base terminal (54) and emitter terminal (55) of the transistor **mounted** on the **mounting** substrate (50). The collector connector (57), back connector (58) and emitter connector (59) connects the respective terminals and **electrodes** of the transistor.

ADVANTAGE - Avoids provision for **wiring** and package. **Mounts** directly without providing recess. Facilitates quality judgment about fusion of connector by observation from back side.
Dwg.1/8

L34 ANSWER 19 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1995-112112 [15] WPIX

CR 1995-126813 [17]; 1995-126814 [17]

DNN N1995-088241

TI Structure of probe apparatus - uses movable plate below which multilayer **wiring** board is provided having many bumps which are contacted with **electrode** pad on **wafer** placed on stand.

DC S01 U11

IN SANO, K

PA (TKEL) TOKYO ELECTRON LTD; (TKEL) TOKYO ELECTRON YAMANASHI LTD

CYC 2

PI JP 07037943 A 19950207 (199515)* 5p

US 5559446 A 19960924 (199644) 14p

US 5982183 A 19991109 (199954)

JP 3103957 B2 20001030 (200057) 4p

ADT JP 07037943 A JP 1993-200023 19930719; US 5559446 A US 1994-276847 19940718; US 5982183 A Cont of US 1994-276847 19940718, US 1996-655485 19960530; JP 3103957 B2 JP 1993-200023 19930719

FDT US 5982183 A Cont of US 5559446; JP 3103957 B2 Previous Publ. JP 07037943

PRAI JP 1993-200023 19930719; JP 1993-212214 19930803; JP 1993-212215 19930803

AB JP 07037943 A UPAB: 20001109

The probe apparatus has a stand (2) on which a **wafer** (W) to be inspected is **mounted**. A movable plate (4) attached to a **link** arm (43) is placed above the **wafer**. A flexible

multilayer **wiring** board (31) having many bumps (32) is attached to the under surface of the movable plate. Both ends of the flexible multilayer **wiring** board are fixed to an upper PCB. The multilayer **wiring** board is pressed below with a buffer (44) through a notch (41) provided at the movable plate. The bump of the multilayer **wiring** board is contacted with **electrode** pad of the **wafer** and inspection is performed.

USE/ADVANTAGE - For use in measuring input-output characteristics of **integrated circuit chip** after packaging is carried out. Performs measurement with high accuracy. Reduces wear of conductive protrusion.

Dwg.1/4

L34 ANSWER 20 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1994-295505 [37] WPIX

DNN N1994-232545

TI Packaged semiconductor device esp. with flip-**chip** bonded **integrated circuit** for microstrip line mounting - has IC back **electrode** electrically connected to package metallic cap.

DC U11

IN SHIGA, N

PA (SUME) SUMITOMO ELECTRIC IND CO

CYC 7

PI EP 615289 A2 19940914 (199437)* EN 18p
R: DE FR GB SE

CA 2118785 A 19940911 (199443)

JP 06268020 A 19940922 (199443) 8p

EP 615289 A3 19950412 (199544)

US 5723904 A 19980303 (199816) 16p

ADT EP 615289 A2 EP 1994-400530 19940310; CA 2118785 A CA 1994-2118785 19940310; JP 06268020 A JP 1993-76104 19930310; EP 615289 A3 EP 1994-400530 19940310; US 5723904 A US 1994-208267 19940310

PRAI JP 1993-76104 19930310

AB EP 615289 A UPAB: 19941109

The packaged semiconductor include an insulating substrate, with multiple connection pads (6) formed on an upper surface and multiple external connections (7) formed on another, lower surface. Corresp. external connections and connection pads are coupled through via **holes** in the insulating substrate (2). An **integrated circuit** is bonded face down on the substrate upper surface, so that the IC is **electrically connected** to the **pads** through **solder** bumps (9).

An electrically conductive cap (3) covers the insulating substrate upper surface, so that the IC is encapsulated between the substrate and the cap. The IC back **electrode** is **electrically connected** to the cap e.g. by a contact plate with a central region mechanically and **electrically connected** to the IC back **electrode**. Pref. the cap includes a sidewall bonded at its lower end to the substrate, with a lid plate bonded to the sidewall upper end, and the contact plate has an **edge** sandwiched and electrical connected between the lid and the side plate. The contact plate may be a lead frame.

ADVANTAGE - Maintains HF performance of IC; prevents conductive solder flowing within package; efficient solder use.

Dwg.2/8

L34 ANSWER 21 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1994-226956 [28] WPIX

04/10/2002

Serial No.:09/852,847

DNN N1994-178914

TI Spark plug voltage detector for use with internal combustion engine - has
electrode plate embedded in insulator body
electrically connected to lead, **wire** with pair
of insulator plates located adjacent to body, each having **groove**
for receiving spark plug cable.

DC Q54 S01 S02 X22

IN KONDO, N; MIYATA, S

PA (NITS) NGK SPARK PLUG CO LTD

CYC 5

PI EP 607035 A2 19940720 (199428)* EN 10p

R: DE FR GB IT

US 5450013 A 19950912 (199542) 9p

EP 607035 A3 19950412 (199544)

EP 607035 B1 19970402 (199718) EN 11p

R: DE FR GB IT

AB EP 607035 A UPAB: 19940831

The detector comprises an **electrode plate** (21)
embedded in an insulator body (2) which is **electrically**
connected to a lead **wire** (22). A pair of plates (31 and
32) are located adjacent to the insulator body. Each plate has a
groove (33 and 34) receiving a spark plug cable (Hc) of the
secondary **circuit**.

A pair of electromagnetic shield plates (4 and 5) sandwich the
insulator body and the pair of plates (31 and 32). The pair of plates are
insulators. The electromagnetic shield plates are bolted (6) together, the
bolt forming the electrical connection for the plates, which are formed of
aluminium or an alloy of aluminium.

ADVANTAGE - Detector allows easy separate replacement of components,
and precisely detects characteristics of spark plug voltage waveform
applied to each spark plug **mounted** on cylinders with a
relatively simple structure.

Dwg.2/5

L34 ANSWER 22 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
 AN 1994-122155 [15] WPIX
 DNN N1994-261806
 TI Tape carrier package type semiconductor device capable of preventing crosstalk - has semiconductor **chip** disposed in **hole** made in insulating film, and **wiring** pattern having leads formed on one of top and bottom surfaces of insulating film, each with lead connected to **chip**.
 DC U11
 IN IKEMIZU, M; OKUTOMO, T
 PA (TOKE) TOSHIBA KK
 CYC 3
 PI JP 06069275 A 19940311 (199415)* 12p
 US 5359222 A 19941025 (199442)B 17p
 US 5659198 A 19970819 (199739) 18p
 KR 9704217 B1 19970326 (199937)
 ADT JP 06069275 A JP 1992-328893 19921114; US 5359222 A US 1993-11133 19930129; US 5659198 A Div ex US 1993-11133 19930129, Cont of US 1994-212875 19940315, US 1995-539737 19951005; KR 9704217 B1 KR 1993-1224 19930130
 FDT US 5659198 A Div ex US 5359222
 PRAI JP 1992-17097 19920131
 AB US 5359222 A UPAB: 19941212 ABEQ treated as Basic
 The inner lead portion of each of the leads is bonded to a corresp one of **bump electrodes** formed on pads of a semiconductor **chip** and the outer lead portion thereof is connected to a corresp lead **wire** formed on a printed **circuit** board. The outer lead portion of one of the leads which acts as a ground **line** is connected to a grounded lead **wire** which is formed on the printed **circuit** board. An insulating adhesive agent bonds a shield plate to the under surface of the **wiring** pattern.
 The semiconductor **chip** is **mounted** on a base plate having a number of lead **wires** connected to the outer lead portions. At least one of the number of lead **wires** is grounded and **electrically connected** to the shield plate. The lower surface of the shield plate and the connections of the lead **wires** to the outer lead portions are in the same plane. The semiconductor **chip** and the inner lead portions are hermetically sealed by use of potting resin.

L34 ANSWER 23 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
 AN 1991-271498 [37] WPIX
 DNN N1993-164874 DNC C1993-095174
 TI Mfg. process for DRAMs with **trench** construction - forms primary dielectrics in **trench** before polycrystalline silicon is doped in N-type impurity NoAbstract Dwg 1/6.
 DC L03 U11 U13 U14
 IN KIM, C; LEE, J; KIM, C S; KIM, D Y; LEE, J H; LEE, K H
 PA (KANK-N) KANKOKU DENSHI TSUS; (KOEL-N) KOREA ELEC & TELECOM RES INST; (ELTE-N) ELECTRONICS & TELECOM RES
 CYC 3
 PI JP 03180066 A 19910806 (199137)*
 KR 9204368 B 19920604 (199307)
 US 5223447 A 19930629 (199327)B 12p
 ADT JP 03180066 A JP 1990-229535 19900829; KR 9204368 B KR 1989-12747 19890904; US 5223447 A US 1990-577109 19900904

04/10/2002

Serial No.:09/852,847

PRAI KR 1989-12747 19890904

AB JP 03180066 A UPAB: 19960705

A mask for forming outer **electrode** has two **stacked plates**, recesses formed in surface of the plates for holding and positioning **chip** type unit, and opening formed on the plates and overlapped to the recess.

ADVANTAGE - When the **chip** unit is held between the plates a part of surface of the unit is exposed to the opening, and by sputtering or ion plating, the outer **electrode** can be formed. Further, since accuracy of size is improved, dispersion of electric property of the unit can be reduced. @(6pp Dwg.No.1,2/6)@

L34 ANSWER 24 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1990-209990 [28] WPIX

DNN N1990-163265

TI **Electrode plate** structure with layers of active material - has forces or perforations through active material and embossments between last two facing surfaces which are compressed together.

DC X16 X22

IN WITEHIRA, P

PA (WITE-I) WITEHIRA P; (ZEHN-I) ZEHNER H

CYC 26

PI AU 8928969 A 19900531 (199028)*

EP 370534 A 19900530 (199031)

AB AU 8928969 A UPAB: 19950524

The **electrode plate** structure consists of layers of active material either in sheet form or pasted mass form and having pores and/or perforations throughout the active material and having corrugations, **ridges**, **grooves**, furrows, creases or other embossments between at least two facing surfaces which are compressed together.

The corrugations, **ridges**, **grooves**, furrows, creases provide pathways along which electrolyte may flow in tandem with diffusion through perforations and/or pores of the structure, thereby allowing electrolyte penetration to deep within the structure at a flow rate that allows correct electrochemical reactions by reason of layers or laminations being **electrically connected** as one body. Sheet material is able to be formed by rolling, pressing, casting, cutting or moulding in tandem or simultaneously. Solid or absorbed electrolyte is compressed between layers.

L34 ANSWER 25 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1990-157516 [21] WPIX

DNN N1990-122436

TI Capacitance type accelerometer for motor vehicle - has thermal oxide films disposed between silicon **plates** except **electrode** part.

DC S02 U12 X22

IN MATSUMOTO, M; MIKI, M; SUZUKI, S; TSUCHITANI, S

PA (HITA) HITACHI LTD

CYC 5

PI EP 369352 A 19900523 (199021)*

R: FR GB

AB EP 369352 A UPAB: 19971021

The capacitance type accelerometer has a first silicon plate (2, 7) formed as having a movable **electrode** part (7) which is moved according to acceleration, two second silicon plates (1, 3) which are disposed on

04/10/2002

Serial No.:09/852,847

both sides of the first silicon plate with a certain separation distance. Thermal oxide films (4, 5) which are respectively disposed between the first silicon **plate** except the movable **electrode** part (7) and the two second silicon plates (1, 3) and stick the first silicon plate 8(3) except the movable **electrode** and the two second silicon plates together.

The process of manufacturing the capacitance type accelerometer is made by processing and cutting a water by dicing saw without coming into the accelerometer of cutting **chips** or cutting water.

USE/ADVANTAGE - For engine control. Enhanced detection accuracy.

L34 ANSWER 26 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD
AN 1989-000753 [01] WPIX

DNN N1989-000653

TI Laminated electrical capacitor with inbuilt safety function - has **plates** formed with **electrodes** and terminal section coupled by fused **links**.

DC V01

IN MORI, S; MURATA, K

PA (MURA) MURATA MFG CO LTD

CYC 3

PI DE 3819255 A 19881222 (198901)* 9p
JP 63305505 A 19881213 (198904)
JP 63305506 A 19881213 (198904)
US 4894746 A 19900116 (199010) 8p

AB DE 3819255 A UPAB: 19930923

An electrical capacitor is formed around a dielectric laminated **stack** of elements (12a,12b,12c). The dielectric layers (12b) carry a series of **electrodes** (17), as do the other dielectric layers (12c). Each of the internal **electrodes** forms a capacitive region (19) and a terminal section (20). Between the two regions is a fused connecting **link** (21). A similar arrangement (18,23,24) is provided for the other plates.

The plates are **stacked** by alternating. The capacitive regions and terminal sections are formed by printing with a film formed of a metal paste. End laminates complete the **stack** which is then built into a housing.

L34 ANSWER 27 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1987-125771 [18] WPIX

DNN N1990-202347 DNC C1987-052329

TI Bump **chip mounting** structure - connects central **bumps** to substrate terminal **electrode** via **bump** connecting pad NoAbstract Dwg 1/9.

DC U11 V04

PA (SHAF) SHARP KK

CYC 2

PI JP 62067829 A 19870327 (198718)* 20p
US 4949224 A 19900814 (199035)

ADT JP 62067829 A JP 1985-209086 19850920; US 4949224 A US 1988-233843
19880816

PRAI JP 1985-209085 19850920; JP 1985-209086 19850920

L34 ANSWER 28 OF 62 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 1983-802957 [44] WPIX

DNN N1983-193623

TI Strip-type piezoelectric resonator mfr. - has conductive layer at

chip plate ends directly **mounted** on base for electrical connection to **electrodes**.

DC V06
 IN FUJIIWARA, Y; HOSHINO, H; KOJIMA, Y; YAMADA, S
 PA (FUIT) FUJITSU LTD
 CYC 5
 PI EP 92428 A 19831026 (198344)* EN 30p
 R: DE FR GB
 JP 58182911 A 19831026 (198349)
 JP 58190110 A 19831107 (198350)
 US 4757581 A 19880719 (198831)
 EP 92428 B 19900404 (199014) EN
 R: DE FR GB
 DE 3381424 G 19900510 (199020)
 ADT EP 92428 A EP 1983-302211 19830419; US 4757581 A US 1986-938457 19861205
 PRAI JP 1982-65947 19820420; JP 1982-72451 19820428
 AB EP 92428 A UPAB: 19930925

A strip-type energy trapping resonator **chip** (22) is **mounted** on a base **plate** (24), with **electrode** patterns (27,27') on opposite main surfaces. One main surface of the **chip** plate faces and is parallel with the base. A conductive layer is formed on each end of the main surface facing the base plate, the thickness of the conductive layer being greater than that of the **electrode** pattern, so that the pattern is separated from the base plate.

The conductive layers are directly **mounted** on conductive parts of the base plate, to **electrically connect** the **electrode** patterns and the conductive parts of the base plate. A cap (23) seals the resonator **chip** onto the base plate. The construction replaces pairs of support **wires**, which occupy a relatively large space.

3/33

L34 ANSWER 29 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 2001-250886 JAPIO
 TI **WIRING SUBSTRATE**
 IN OKUBO RIICHI
 PA TOPPAN PRINTING CO LTD
 PI JP 2001250886 A 20010914 Heisei
 AI JP2000-063544 (JP2000063544 Heisei) 20000308
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
 AB PROBLEM TO BE SOLVED: To provide a **wiring** subfastrate having a flip-**chip** connection terminal where enough junction strength to a **bump electrode** of a semiconductor **chip** can be obtained when a semiconductor **chip** is joined to a **wiring** substrate.
 SOLUTION: On a **wiring** substrate 100, a **wiring** layer 12 and a flip-**chip** connection terminal 13 are formed on an insulating base material 11, and the flip-**chip** connection terminal 13 is formed by forming a 1 μ m or more thick silver film on the copper metal and furthermore, the silver film is formed by electrolytic silver plating with a current density of 1 to 50 A/dm². A semiconductor **chip** mount part 15 is formed in a central part of the **wiring** substrate 100, a **wiring** layer 17 and a solder bump 18 are formed in a rear, and the **wiring** layer 12 and the **wiring** layer 17 are **electrically connected** through a **via hole** 14.
 COPYRIGHT: (C)2001,JPO

L34 ANSWER 30 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 2001-044359 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE, THE SEMICONDUCTOR DEVICE,
MOUNTING SUBSTRATE AND ELECTRONIC DEVICE
IN MAKABE AKIRA; SATO HIDEKAZU
PA SEIKO EPSON CORP
PI JP 2001044359 A 20010216 Heisei
AI JP1999-218953 (JP11218953 Heisei) 19990802
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To **stack** semiconductor **chips** of similar sizes.
SOLUTION: Plural device **holes** 14 (14A and 14B), on which semiconductor **chips** 18 (18A and 18B) are **mounted** and which are formed into columnar shapes and an outer connection **electrode** 16 which is connected in the forming direction of the device **holes** 14 and is **electrically connected** to the semiconductor **chips** 18 via a metallic **wiring** 24, are installed in the inner side of a flexible substrate 12. When a device is bent along bend **lines** 30, which are set between the device **holes** 14 and between the device **hole** 14 and the outer connection **electrode** 16, the semiconductor **chips** 18 can be overlapped on the outer connection **electrodes** 16, where **solder balls** 26 are **mounted**. Thus, the functions of the semiconductor device 10 itself can be increased without having to change the **mounting** area. Then, a **mounting** substrate can be miniaturized by making the device 10 multifunctional, and an electronic unit using the **mounting** board can be also miniaturized.
COPYRIGHT: (C)2001,JPO

L34 ANSWER 31 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 2001-035865 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN TAKESHITA TATSUO; SAKAKIBARA MASAYUKI
PA HAMAMATSU PHOTONICS KK
PI JP 2001035865 A 20010209 Heisei
AI JP1999-203549 (JP11203549 Heisei) 19990716
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001
AB PROBLEM TO BE SOLVED: To provide the manufacturing method of semiconductor devices, which suppresses the occurrence of remaining air when an insulative resin is filled in the gap between a semiconductor substrate and a packaging board and can suppress a reduction in the reliability of the semiconductor devices.
SOLUTION: A second through **hole** 26 is formed in almost the central part, which corresponds to almost the central part of a region formed with a plurality of semiconductor **chips** 1 on a semiconductor substrate 10, of a packaging board 20, the substrate 10 is **mounted** on the board 20 in a state such that a gap 30 of a prescribed width is formed between the substrate 10 and the board 20, first **wiring electrodes** 21 and **bumps** 13 are **electrically connected** with each other, the substrate 10 and the board 20 are integrally constituted, and an underfill resin is filled in the gap 30 through the **hole** 26. After the underfill resin 31 is filled in the gap 30 and is cured, the substrate 10 and the board 20 are cut integrally across through **holes** 25, and the substrate 10 and the board 20 are respectively separated into the plurality of the **chips** 1 and a plurality of package bases 2 to form individual semiconductor devices A.
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L34 ANSWER 32 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 2000-340692 JAPIO
TI **WIRING BOARD, SEMICONDUCTOR DEVICE, ELECTRONIC DEVICE AND MANUFACTURE THEREOF**
IN ONDA MAMORU; MURAKAMI HAJIME; KASHIWABARA FUMITAKA
PA HITACHI CABLE LTD
PI JP 2000340692 A 20001208 Heisei
AI JP1999-146255 (JP11146255 Heisei) 19990526
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To reduce manufacturing process and cost by attaching a material for buffering thermal stress occurring in a semiconductor **chip** and an insulating basic material to the entire surface of the insulating basic material except the **electrode pad** region of the semiconductor **chip** on the side for **mounting** the semiconductor **chip**.
SOLUTION: An elastomer 70 buffers thermal stress occurring due to difference in the coefficient of thermal expansion between a semiconductor **chip** 30 and a tape substrate 10. The semiconductor **chip** 30 is attached onto the elastomer 70, the **electrode pads** 50 of the semiconductor **chip** 30 exposed from a ribbon lead connecting slit 80 are **connected electrically** with a **wiring pattern** 40 through ribbon leads 81 and **solder balls** 20 are formed in the **solder ball holes** 90 on the **wiring pattern** 40 on the side opposite to the connecting side with the semiconductor **chip** 30. Since a metal **link** having coefficient of thermal expansion identical to that of the tape substrate is not required, manufacturing cost of the semiconductor device can be reduced.
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L34 ANSWER 33 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 2000-068313 JAPIO
TI SEMICONDUCTOR **CHIP** AND SEMICONDUCTOR DEVICE USING THE SAME
IN ANDO HIDEKO; KIKUCHI HIROSHI; YOSHIDA IKUO; SATO TOSHIHIKO
PA HITACHI LTD
PI JP 2000068313 A 20000303 Heisei
AI JP1998-246523 (JP10246523 Heisei) 19980818
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000
AB PROBLEM TO BE SOLVED: To increase effective area of solder bump arrangement.
SOLUTION: **Electrode** contacting openings 17 are opened on a shielding film 16, that coats the main surface of an active region 11 side of a semiconductor **chip** 10, solder bumps 12 are protruded at positions apart from the **electrode** contacting openings 17, and the solder bumps 12 are **electrically connected** to the **electrode** connecting openings 17 with electrical **wiring** 18 laid on the surface of the shielding film 16. Height h of the solder bumps 12, distance L between the **edge** of a solder **bump** 12 and an **electrode** connecting opening 17, opening width a of the **electrode** connecting opening 17, and thickness t of the shielding film are designed so as to satisfy the inequality $(h/L) \leq (t/a)$. As a result of this, since the failure of a memory cell due to α -ray infiltrating from an **electrode** connecting opening can be prevented, because the α -ray from the solder bump inside can be prevented from being introduced into the inside of the **chip**. In a C4 **mounting** structure of a memory **chip**, since the latitude in solder bump layout can be increased, memory **chip** or the area of a semiconductor device using the same

can be reduced.

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L34 ANSWER 34 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 2000-067931 JAPIO

TI SECONDARY BATTERY

IN IWAZONO YOSHINORI; MASUMOTO KANEHITO

PA MATSUSHITA ELECTRIC IND CO LTD

PI JP 2000067931 A 20000303 Heisei

AI JP1998-238324 (JP10238324 Heisei) 19980825

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000

AB PROBLEM TO BE SOLVED: To prevent an electrolyte from leaking outside by providing an assembled sealing plate with a filter connected to one **electrode** through a lead **plate**, a sub-filter coming into surface contact with the filter, a valve body formed of a metal thin plate to be ruptured by a predetermined pressure, a valve body rupturing ring, and a flexible **wiring** board on which a safety **circuit** **electrically connected** to the filter is **mounted**

SOLUTION: A cylindrical lithium battery has a filter 48, a sub-filter 49, a valve body 47, and a valve body rupturing ring 46. Explosion-proofing slits G are formed in the valve body 47, which is welded to the filter 48. An electrolyte gasified by heat generation pushes up the valve body 47 toward a safety **circuit** side through **holes** H of the filter 48. At that time, the pressure of the gas ruptures the slits G formed in the valve body 47, and thereby, the gas is released outside through a **hole** E formed in the safety **circuit**, **holes** I formed in the controlled positive input and output, and **holes** J formed in a safety **circuit**-use negative **electrode**, so that an explosion-proof measure is accomplished.

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L34 ANSWER 35 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 2000-012584 JAPIO

TI SEMICONDUCTOR DEVICE, ITS MANUFACTURE AND IC CARD

IN TSUNODA SHIGEHARU; HOZOJI HIROYUKI; SAEKI JUNICHI; ENDO TSUNEO

PA HITACHI LTD

PI JP 2000012584 A 20000114 Heisei

AI JP1998-178657 (JP10178657 Heisei) 19980625

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2000

AB PROBLEM TO BE SOLVED: To realize a semiconductor device of low cost which is thinned, has high reliability and high dimensional precision (especially, thickness direction), and can be **mounted** on an IC card or the like.

SOLUTION: A semiconductor device 50 is provided with a **wiring** board 2 where a plurality of thin **plate** type **electrodes** are arranged, and fixed so as to constitute connecting terminals on a single side of an insulating board 2' where a **hole** 5 for **mounting** is bored at a part **mounting** a semiconductor element 1; the semiconductor element 1 which is **mounted** and fixed on a thin **plate** type **electrode** in the **hole** for **mounting** of the insulating board on the **wiring** board by using adhesive agent 6; **connecting** means 7 **electrically connecting** a plurality of **electrodes** arranged on a **circuit** surface of the semiconductor element with a plurality of the **electrodes** of the **wiring** board; and a resin sealing part 8 where the insulating board side of the **wiring** board is so resin-sealed and molded, containing at least the semiconductor element 1 and the connecting means,

that a gate trace 9 of resin for sealing is isolated from the insulating board scarcely applying stress to the **wiring** board when a gate is eliminated.

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L34 ANSWER 36 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1999-330159 JAPIO
 TI SEMICONDUCTOR DEVICE
 IN OKAMOTO IZUMI
 PA MATSUSHITA ELECTRIC IND CO LTD
 PI JP 11330159 A 19991130 Heisei
 AI JP1998-131672 (JP10131672 Heisei) 19980514
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
 AB PROBLEM TO BE SOLVED: To improve the yield of connections by forming the pattern of a conductor **wiring**, in a shape having the recess part with the area smaller than the protruding **electrode** of a semiconductor element, and holding this conductor **wiring** with a base material.
 SOLUTION: A conductor **wiring** 2 is formed at the surface of a base material 1 such as glass epoxy by exposure, etching and the like. At this time, the pattern wherein a **hole** 2a as a recess part extending to the bottom is formed in the inside of the conductor **wiring** 2 is formed. Then, the position of this conductor **wiring** 2 and the position of a protruding **electrode** 4 of a semiconductor element 3 comprising solder and the like are aligned and **electrically** and mechanically **connected** by the flip-chip mounting by solder flip-chip. At this time, a part of the protruding **electrode** 4 is made to enter into the **hole** 2a of the conductor **wiring** 2 through the pressure at the time of **mounting**. Thereafter, encapsulating is performed by an encapsulating resin 7. Then, a **solder ball** 6 is **mounted** on a conductor **wiring** 5, and the **electrode** is formed by reflow and the like.
 COPYRIGHT: (C)1999,JPO

L34 ANSWER 37 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1999-121477 JAPIO
 TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
 IN YAMAJI YASUHIRO
 PA TOSHIBA CORP, JP (CO 000307)
 PI JP 11121477 A 19990430 Heisei
 AI JP1997-288646 (JP09288646 Heisei) 19971021
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99, No. 4
 AB PURPOSE: TO BE SOLVED: To obtain **mounting** efficiency degree approximate to degree of bare **chip mounting**, by **electrically connecting chip pad electrodes** and board pad **electrodes** of a **wiring board** which has **electrodes** and board pad **electrode** working as external terminals of an **integrated circuit** and whose outer shape is smaller than that of a semiconductor **chip**, and sealing the **electrodes** from the outside.
 CONSTITUTION: pad **electrodes** are formed on one surface of a semiconductor **chip** 1, arranged along the **edge** of the semiconductor **chip** 1 and **electrically connected** with an **integrated circuit**. A board foot print 22 is formed on the **mounting** surface of a **mounting board** (circuit board) 21. **Bump electrodes** 8 for **mounting** face the **mounting**

surface of the **mounting** board 21 and are connected with the foot print 22 formed on the **mounting** surface, and a desired electric product is constituted. That is, **mounting** to the **mounting** board 21 is enabled as it is, and the size is identical to the outer shape of the **chip** 1. As a result, **mounting** to the **mounting** board 21 is enabled with extremely high **mounting** density, e.g. practical efficiency of degree approximate to bare **chip mounting**.

L34 ANSWER 38 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1998-223795 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR PACKAGE
IN ICHIMURA SHIGEKI; TSUBOMATSU YOSHIAKI; INOUE FUMIO; YUSA MASAMI
PA HITACHI CHEM CO LTD, JP (CO 000445)
PI JP 10223795 A 19980821 Heisei
AI JP1997-19556 (JP09019556 Heisei) 19970203
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 8
AB PURPOSE: TO BE SOLVED:To provide a method of manufacturing a small semiconductor package which is enhanced in reliability by a method wherein the semiconductor package is kept free from cracks by relaxing the inner pressure due to steam generated in reflow taking advantage of a through-hole.
CONSTITUTION: pening 3 and a through-hole 9 are provided to a polyimide bonding sheet 1. A copper foil is stuck, and then an inner connection part and an expansion wiring 2 are formed. A frame is punched out of the sheeting, and openings which are made to serve as inner connection sections, expansion wirings, and outer connection sections are provided to the frame to make it serve as a support board (a). A die bond film is attached to the rear side of a wafer 6, and the wafer 6 is diced into die bond material-attached chips as prescribed in dimensions (b). The die bond material- attached chips 6 are bonded to the semiconductor chip mounting region of the insulating support board, the electrode of the semiconductor chip is electrically connected to the inner connection section (c), the insulating support board mounted with the semiconductor chips 6 is put in a transfer molding die and sealed up with semiconductor sealing epoxy resin (d), a solder ball is arranged at each opening which serves as an outer connecting section and melted (e), and then the supporting board is divided into unit semiconductor packages by punching (f).

L34 ANSWER 39 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1998-189820 JAPIO
TI SUPPORTING SUBSTRATE FOR SEMICONDUCTOR CHIP, SEMICONDUCTOR DEVICE AND MANUFACTURE OF SEMICONDUCTOR DEVICE
IN SODA YOSHIKI; MIYATA KOJI; INOUE FUMIO; YAMAZAKI AKIO; TSUBOMATSU YOSHIAKI; NAKAMURA HIDEHIRO; AWANO YASUHIKO; ICHIMURA SHIGEKI; YUSA MASAMI; IWASAKI YORIO
PA SHARP CORP, JP (CO 000504)
HITACHI CHEM CO LTD, JP (CO 000445)
PI JP 10189820 A 19980721 Heisei
AI JP1997-204547 (JP09204547 Heisei) 19970730
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 7
AB PURPOSE: TO BE SOLVED:To prevent generation of package cracks and to obtain a chip-supporting substrate, with which a small-type semiconductor device can be manufactured, and a semiconductor device.

CONSTITUTION: bstrate, on which a plurality of sets of inner connection parts, expansion wirings 2, aperture parts 3, which become outer connection parts, and through-holes 9 are formed on a polyimide bonding sheet 1, is prepared. (a) A die-bonding film 4 is formed on the chip-mounting region of the substrate, and the die-bond film 4 is adhered using a wiring/metal pattern. (b) A semiconductor chip is adhered to the substrate using non-silver containing paste on the die-bond film 4. At this time, a void, which is connected to the through-holes 9, is formed between the die-bond film 4 and a bonding sheet 1 on the part having no wiring/metal pattern. A chip electrode and an inner connection part are electrically connected by bonding a metal wire 5. (c) The chip electrode and the inner connection part are sealed by sealing an epoxy resin 7. (d) Solder balls 8 are arranged on the aperture part which becomes an outer connection part, and they are connected by fusing. (e) Separation into individual packages are made.

L34 ANSWER 40 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1998-189665 JAPIO
 TI SEMICONDUCTOR DEVICE
 IN SAKAGUCHI SHIGEKI; KAMETAKA MAKOTO
 PA MATSUSHITA ELECTRON CORP, JP (CO 000584)
 PI JP 10189665 A 19980721 Heisei
 AI JP1996-342996 (JP08342996 Heisei) 19961224
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 7
 AB PURPOSE: TO BE SOLVED:To reduce the thickness of a semiconductor device and miniaturize the device by a method wherein the semiconductor device is made to have such a structure that a semiconductor chip is not mounted and held on a board, but surrounded with a tape possessed of conductors.
 CONSTITUTION: miconductor chip 8 is surrounded with a chip-pasted tape 10 equipped with inner leads 9, and electrode pads 11 located on the upside of a semiconductor chip 8 are electrically connected to the exposed parts of the inner leads 9 partly exposed out of the tape 10 with a metal fine wire 12. The exposed upside of the semiconductor chip 8 is sealed up with sealing resin 13. The edges of the inner leads 9 are exposed at the base of the chip-pasted tape 10, and a solder ball 14 is provided to the edge of the inner lead 9 to serve as an outer electrode.
 By this constitution, the semiconductor chip 8 can be held with a tape, so that the thickness of a semiconductor device can be further reduced than a case where a board is employed, and a semiconductor device of thin-type can be realized.

L34 ANSWER 41 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1998-173000 JAPIO
 TI SEMICONDUCTOR PACKAGE FOR HIGH DENSITY MOUNTING AND MOUNTING METHOD THEREOF
 IN TANAKA YASUNORI; HAGIMOTO EIJI
 PA NEC CORP, JP (CO 000423)
 PI JP 10173000 A 19980626 Heisei
 AI JP1996-330678 (JP08330678 Heisei) 19961211
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 6
 AB PURPOSE: TO BE SOLVED:To prevent the damage of a connection part owing to

a thermal expansion difference by means of a temperature change, by arranging **solder ball electrodes** at the back of a package in a grid form, and loading and **electrically connecting solder balls** on/to a printed board by melting/solidifying the **solder balls** fitted to the **solder ball electrodes**.

CONSTITUTION: ring tape 3 is adhered to a semiconductor **chip** 2 as the package. A **solder ball electrodes** 31 being flip **chip mounting electrodes** are formed in the grid form on the side of the back of the **wiring** tape 3. **Wire bonding electrodes** 33 are **electrically connected** to the **solder ball electrodes** 31 by melting and solidifying **solder balls** 32 fitted on the respective **solder ball electrode** 31 in the side **edge** part of the back of the **wiring** tape 3. Thus, the damage to the connection part owing to the thermal expansion difference by the temperature change can be prevented, and fine soldering, **wire** bonding and flip **chip mounting** can be realized.

L34 ANSWER 42 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1998-150273 JAPIO

TI HIGH-DENSITY **MOUNTING BOARD WITH SURFACE ACOUSTIC WAVE ELEMENT CHIP**

IN KANDA TADASHI

PA KOKUSAI ELECTRIC CO LTD, JP (CO 000112)

PI JP 10150273 A 19980602 Heisei

AI JP1996-309626 (JP08309626 Heisei) 19961120

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 6

AB PURPOSE: TO BE SOLVED:To lessen a printed board which is equipped with an acoustic surface wave element **chip** and lessened in size, thickness, and cost.

CONSTITUTION: rst board 21 and a second board 22 are pasted together into a multilayer printed board 20, **wiring** patterns 6 and 24 are provided to the printed board 20, and the **wiring** patterns 6 and 24 are connected together through through-holes 25. A cutout of prescribed size is provided in the board 20, a recess 10 is formed of the cutout and the underside of the first board 21, and first connection pads 26 arranged on the lateral sides, second connection pads 31 connected to the pads 26 with **solder** bumps 32, and an acoustic surface wave device **chip** 12 which is provided with a metal **electrode** pattern formed on its surface and mechanically, **electrically connected** to the connection pads 31 are housed in the recess 10. The acoustic surface wave device **chip** 12 is sealed up with high-viscosity epoxy resin 33 controlled in viscosity so as not to flow into a gap between the first board 21 and the **chip** 12.

L34 ANSWER 43 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1998-065057 JAPIO

TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

IN HIGUCHI KAZUTO; KONNO YOSHIO; KURIYAMA YASUHIKO; ONO NAOKO; SAITO MASAYUKI

PA TOSHIBA CORP, JP (CO 000307)

PI JP 10065057 A 19980306 Heisei

AI JP1996-213409 (JP08213409 Heisei) 19960813

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 3

AB PURPOSE: TO BE SOLVED:To **mount** a semiconductor **chip**

with its face up and reduce the **mounting** area by using a semiconductor **chip** having **bump electrodes** formed on input/output terminals arranged at the marginal area of the **chip** and **electrically connecting** the **bump electrode** side faces to the **wiring electrode** surface on a board with solder bridges.

CONSTITUTION: t/output terminals 9 are formed at the marginal area of a base semiconductor **chip** 2 and **bump electrodes** 4 formed on the terminals 9. A semiconductor **chip** 3 mounted on the **chip** 2 is mounted on a mounting board 1 with a hybrid IC molded with a resin mold 13 and **bump electrodes** 4 **electrically connected** to **wiring electrodes** 11 near the **electrodes** 4 through bridges 5. The side faces of the **electrodes** 4 are **flush** with the side face of the base board 2 and solder bumps formed at the side faces are well connected. Thus it is possible to place the **wiring electrodes** 11 near round the **chip** 2 on the board 1 and reduce the **mounting** area.

L34 ANSWER 44 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1997-307013 JAPIO
 TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE AND MANUFACTURE THEREOF
 IN MITSUI TAKAAKI; NAGATA SATOSHI
 PA MITSUI HIGH TEC INC, JP (CO 325382)
 PI JP 09307013 A 19971128 Heisei
 AI JP1996-116665 (JP08116665 Heisei) 19960510
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 11
 AB PURPOSE: TO BE SOLVED:To provide a high-yield and high-reliability semiconductor **integrated circuit** device easy to **mount** by forming it as an **integrated circuit** substrate, without dicing a substrate formed by slicing a Si single crystalline rod.

CONSTITUTION: ntegrated **circuit** substrate is formed by slicing a Si single crystalline rod having an outline shape with leaving this shape uncut. Elements such as transistors and wirings, etc., are formed on this Si substrate 10, **electrode** pads P1 are arrayed along the marginal **edge** of the element forming surface and large **electrode** pad P0 is formed at the center. This pad P0 is **electrically connected** to a **wiring** pattern 11 on the back surface and element regions through high-concn. diffused regions 15 extending in the thickness direction of the substrate. The pads Pi are connected to **solder balls** S1 to be connectable to external **circuits**.

L34 ANSWER 45 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1997-161926 JAPIO
 TI SEMICONDUCTOR **CHIP** SOCKET
 IN SAITO TAKESHI
 PA HITACHI LTD, JP (CO 000510)
 PI JP 09161926 A 19970620 Heisei
 AI JP1995-315161 (JP07315161 Heisei) 19951204
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 6
 AB PURPOSE: TO BE SOLVED:To surely and **electrically connect** the **electrode** pads of a fitting section and the input/output **electrode** pads of a semiconductor **chip** by providing

positioning recesses for inserting positioning **bump electrodes** provided on the principal plane of the semiconductor **chip** at the prescribed position of the semiconductor **chip** fitting section.

CONSTITUTION: t/output **bump electrodes** 13 provided on the principal plane of a semiconductor **chip** 11 are **electrically connected** to **electrode pads** 3 provided on the bottom face of a fitting section 2 where the semiconductor **chip** 11 is fitted, and they are **electrically connected** to through hole **electrodes** 21 provided on a **mounting board** 20 via lead **wires** 4, **electrode pads** 5, and lead pins 6. Positioning **bump electrodes** 14 are provided on the principal plane of the semiconductor **chip** 11, and positioning recesses 7 are provided on the bottom face of the fitting section 2 for the positioning of the input/output **bump electrodes** 13 of the semiconductor **chip** 11 and the **electrode pads** 3 provided on the bottom face of the fitting section 2. The **electrode pads** 3 and the input/output **bump electrodes** 13 can be **electrically and surely connected**.

L34 ANSWER 46 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1997-153520 JAPIO
TI SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME
IN YAMADA HIROSHI; TOGASAKI TAKASHI; SAITO MASAYUKI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 09153520 A 19970610 Heisei
AI JP1995-313305 (JP07313305 Heisei) 19951130
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 6

AB PURPOSE: TO BE SOLVED:To improve the reliability of a flip-**chip mounted** semiconductor by improving the method of inspecting a semiconductor **chip**.
CONSTITUTION: ugh holes are formed on a thermosetting resin sheet 6 on a **wiring pattern** 7 to connect between a semiconductor **chip** 1 formed with **bump electrodes** 3 and the thermosetting resin sheet 6 formed with the **wiring pattern** 7 that is the same in the pattern of **circuit wiring**. Through the through holes, the **bump electrodes** 3 and the **wiring pattern** 7 are connected, using the **wiring pattern** 7 as the **electrodes** for inspection, the semiconductor **chip** 1 is inspected and the connecting **electrodes** 15 of a **circuit wiring board** 14 and the **bump electrodes** 3 are **connected electrically and mechanically**.

L34 ANSWER 47 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1997-115956 JAPIO
TI SEMICONDUCTOR DEVICE
IN TERAJIMA KAZUHIKO
PA CITIZEN WATCH CO LTD, JP (CO 000196)
PI JP 09115956 A 19970502 Heisei
AI JP1995-272212 (JP07272212 Heisei) 19951020
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 5
AB PURPOSE: TO BE SOLVED:To obtain a device with superb cooling property and less noise by providing a substrate **electrode** connected to each **electrode** of a **chip** to be **mounted** on the front of an insulation substrate, a ball terminal connected to a mother board on

the rear, and an electrical path for leading the substrate **electrode** to the **ball** terminal and a member for guiding heat on the upper surface of a **chip** to a ball terminal. CONSTITUTION: bstrate **electrode** 3 and an insulation film 5 are provided on the front of a **wiring** insulation substrate 6, a pad **electrode** 4 and the insulation film 5 are provided on the rear, and further the front substrate **electrode** 3 and the rear pad **electrode** 4 are **electrically connected** via a through hole. Also, a cooling pattern 13 and a thermal core 2a are provided as heat conduction members for reaching from front to rear on the substrate 3. A **chip** 7 is **mounted** on the substrate 6, each **electrode** of an active element surface is guided to the substrate **electrode** 3, heat from an upper part is guided to the substrate 6 by a heat conduction board 12 and a heat conductive adhesive 9a, and each is guided to a mother board through a ball terminal 10 and a cooling terminal 10a, thus obtaining a device with improved cooling property and less noise.

L34 ANSWER 48 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1997-097818 JAPIO
 TI FLIP **CHIP** STRUCTURE AND ITS **MOUNTING** METHOD
 IN HOSHINO KOICHI; MATSUGAYA KAZUOKI
 PA DENSO CORP, JP (CO 000426)
 PI JP 09097818 A 19970408 Heisei
 AI JP1995-277116 (JP07277116 Heisei) 19950928
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 4
 AB PURPOSE: TO BE SOLVED:To prevent lowering of a characteristic of an element in flip **chip mounting**.
 CONSTITUTION: ngs 106, 107, 108 consisting of Au and a multilayer film or the like containing it are formed on the surface 102a of a **circuit chip** 102 by a method such as metal lift-off and plating. On the surface 101a of a substrate 101, wirings 103, 104, 109, 110, 111 consisting of Au and multilayer film containing it constituting a peripheral **circuit** are formed by a method such as metal lift-off (a). The **wiring** 107 is **electrically connected** to **electrodes** for **bumps** 116, 117 formed on the back 102b through conductors inside through **holes** 112, 113 formed on the **circuit chip** 102. The **electrodes** for **bumps** 116, 117 are **electrically connected** to the wirings 104, 110 through bumps 114, 115 such as of Au-Sn solder (b).

L34 ANSWER 49 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1997-074148 JAPIO
 TI MULTI-**CHIP** MODULE AND MANUFACTURE
 IN FUKUOKA YOSHITAKA
 PA TOSHIBA CORP, JP (CO 000307)
 PI JP 09074148 A 19970318 Heisei
 AI JP1995-227987 (JP07227987 Heisei) 19950905
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 3
 AB PURPOSE: TO BE SOLVED:To provide a multi-**chip** module that copes with the global environmental problem as the pollution by lead or the pollution of the air, and the method of manufacturing.
 CONSTITUTION: lti-**chip** module is provided with an inorganic multi-layer **wiring** board 6, a semiconductor element 7 that is **mounted** on the surface of the multi-layer **wiring** board 6 in face down type and a metal cap 9 that seals the semiconductor element inside and the **edge** end of the opening of it is hermetically

sealed to the surface of the multi-layer wiring board 6, and the semiconductor element 7 is provided with bump 7b on the surface of an electrode 7a. The bump 7b is press-fit and fixed to a conductive paste layer 10 that is prepared on the surface of a conductive pad 6a on the multi-layer wiring board 6, electrically connected and mounted, and the metal cap 9 is hermetically sealed with the irradiation of a laser beam.

L34 ANSWER 50 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1996-306820 JAPIO
TI SEMICONDUCTOR DEVICE, PACKAGE FOR SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN SUZUKI KATSUNOBU; SUZUKI KATSUHIKO; HAGA AKIRA; TANMACHI ISAMU; UCHIDA HIROYUKI
PA NEC CORP, JP (CO 000423)
PI JP 08306820 A 19961122 Heisei
AI JP1995-127395 (JP07127395 Heisei) 19950428
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 11
AB PURPOSE: To manufacture a semiconductor device excellent in humidity resistance, reliability and electric performance.
CONSTITUTION: A polyimide layer 13 and copper foil patterns 15, 17 are formed on plate type metal bases 14, 18, and a lamination structure body is constituted. The metal bases are constituted of a ground pattern 14 maintained at the earth potential and many land patterns 18 where solder balls 19 for mounting are formed. The copper foil patterns consist of an island pattern 15 where an LSI 11 is mounted and inner wiring 17 connected with the electrodes of the LSI chip 11. The metal base patterns 14, 18 are electrically connected with the internal wiring 17 via through-holes 22 formed by electroplating. A cap 12 covers the LSI 11 and the wiring pattern 17, and is bonded to the lamination structure body, thereby hermetically maintaining the internal space. A semiconductor device excellent in electric reliability and performance can be manufactured.

L34 ANSWER 51 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1996-064721 JAPIO
TI BALL GRID ARRAY PACKAGE FOR MULTICHIP MODULE AND ITS MANUFACTURE
IN YAMAMOTO SHUJI
PA SUMITOMO METAL MINING CO LTD, JP (CO 329023)
PI JP 08064721 A 19960308 Heisei
AI JP1994-201817 (JP06201817 Heisei) 19940826
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 3
AB PURPOSE: To enable a rework and the assembly at a low cost without the deterioration of the high speed response and the high density wiring by a method wherein outer ball electrodes made of solder and a ceramic or metallic lid which covers the MCM mounted on a single layer ceramic board are provided.
CONSTITUTION: A multichip module(MCM) board 7, hereinafter referred to as MCM, on which a plurality of LSI chips 6 are mounted is bonded to a single layer ceramic board 1 having a number of through-holes 2 whose both ends are to be electrically connected. Further, the outer ball electrodes 13 of the solder filling the through-holes 2 and a ceramic or metallic lid 10 which covers the MCM mounted on the single layer ceramic board are provided. As MCM is mounted not on a multilayer ceramic board but on the single layer ceramic board 1, the cost of the ceramic board can be as low as 1/4 of the conventional cost. On the

other hand, the high speed response and the high density **wiring** which are characteristics of MCM are not deteriorated.

L34 ANSWER 52 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1995-106470 JAPIO
 TI SEMICONDUCTOR DEVICE
 IN KIKUCHI MASAOKI
 PA TOSHIBA CORP, JP (CO 000307)
 IWATE TOSHIBA ELECTRON KK, JP (CO 490850)
 PI JP 07106470 A 19950421 Heisei
 AI JP1993-242883 (JP05242883 Heisei) 19930929
 SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 4
 AB PURPOSE: To provide an aluminum-cap package-type semiconductor device whose thermal resistance is low and which can relax restrictions on reduction of thickness and on miniaturization.
 CONSTITUTION: The title semiconductor device is provided with an aluminum cap 11 which has a leg part 11b at the peripheral **edge** of a nearly square flat- boardlike ceiling part 11a, with an insulator 12 which is bonded to the inner face side of the aluminum cap, with **wiring** patterns 13 which are bonded to the surface of the insulator a plurality of which are installed up to a part near the tip of the leg part of the aluminum cap from the ceiling part of the aluminum cap and which are **connected electrically** to printed-wiring parts on a printed-wiring board 15 on which outer lead parts 13b are to be **mounted** and with **bump electrodes** 10a on the surface side. Then, the title semiconductor device is provided with a semiconductor **chip** 10 in which the **bump electrodes** are bonded to inner lead parts 13a for the **wiring** patterns and with a sealing agent 14 which seals the formation face of the **bump electrodes** for the semiconductor **chip** and bonding parts of the **bump electrodes** to the inner lead parts.

L34 ANSWER 53 OF 62 JAPIO COPYRIGHT 2002 JPO
 AN 1994-260530 JAPIO
 TI SEMICONDUCTOR **INTEGRATED CIRCUIT**
 IN TANAKA HIDEKI; YAMADA MUNEHITO
 PA HITACHI LTD, JP (CO 000510)
 PI JP 06260530 A 19940916 Heisei
 AI JP1993-47743 (JP05047743 Heisei) 19930309
 SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1643, Vol. 18, No. 658, P. 163 (19941213)
 AB PURPOSE: To improve the **mounting** density of a semiconductor **chip** compared with a surface-mount package and a tape carrier package by directly connecting the semiconductor to a **wiring** on a **mounting** substrate.
 CONSTITUTION: A large number of wirings 2, in which, for instance, a Cu foil stuck to this **mounting** board 1 is patterned by etching, are provided on one face of the **mounting** board 1 consisting of epoxy resin impregnated with glass fibers or the like. Further, a rectangular opening holes 3 is provided about in the center of the **mounting** board 1 and the respective one ends of the wirings 2 are arranged so as to project inside this opening 3. And the one ends of these wirings 2 are extended on the bonding pad of a semiconductor **chip** 4 arranged inside this opening 3 and **electrically connected** to the bonding pad through a **bump electrode**. Thereby, a large number of semiconductor **chips** 4 can be **mounted**.

L34 ANSWER 54 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1993-267392 JAPIO
TI MULTILAYER INTERCONNECTION BOARD
IN KAWAHITO MICHIOYOSHI; KAWAI AKINARI
PA HITACHI LTD, JP (CO 000510)
PI JP 05267392 A 19931015 Heisei
AI JP1992-62288 (JP04062288 Heisei) 19920318
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1494, Vol. 18, No. 35, P. 9 (19940119)
AB PURPOSE: To extend the break life of an **electrode** by preventing the occurrence of a thermal stress and a thermal strain at the time of the solder flow, in a thin-film multilayer interconnection board wherein a semiconductor **chip** is connected through **solder balls**.
CONSTITUTION: **Electrodes** for mounting a semiconductor ball are located symmetrically about the center of a thin-film multilayer interconnection board 3 or about the center **line**. These **electrodes** include effective **electrodes** (white circle 4) which are **electrically connected** to a semiconductor **chip** (requiring connection) and uneffective (dummy) **electrodes** (black circle 7). The effective **electrodes** include isolated **electrodes** 6 (having no effective **electrode** at adjacent lattice points). All these **electrodes** are symmetrized (about a point or about a **line**) and are **electrically connected** to a **wiring** on the rear face of the substrate via a through **hole** and therefore electrical isolation of the **electrodes** can be avoided.

L34 ANSWER 55 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1993-102621 JAPIO
TI CONDUCTIVE PATTERN
IN KUBOTA MIYUKI
PA NIPPON CHEMICON CORP, JP (CO 328741)
PI JP 05102621 A 19930423 Heisei
AI JP1991-289267 (JP03289267 Heisei) 19911008
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1417, Vol. 17, No. 453, P. 156 (19930819)
AB PURPOSE: To avoid crossing of conductive patterns without utilizing a jumper **wire** or a through **hole** in a printed **wiring** plate.
CONSTITUTION: When a conductive pattern is formed on a printed **wiring** plate 4, a solder pat 1 for connecting the **electrodes** of the **chip** parts 5 while keeping in touch with a first conductive pattern 2 is divided into two subpats, a second conductive pattern 3 not **electrically connecting** to the first conductive pattern 2 is formed so as to pass through between aforesaid halved solder pats 1, 1 and it is coated with a solder resist layer 8. Then, the **chip** parts 5 are **mounted** and aforesaid halved **solder pads** 1, 1 are **electrically connected**.

L34 ANSWER 56 OF 62 JAPIO COPYRIGHT 2002 JPO
AN 1992-061151 JAPIO
TI SEMICONDUCTOR DEVICE
IN SAWARA KUNIZO
PA HITACHI LTD, JP (CO 000510)
PI JP 04061151 A 19920227 Heisei
AI JP1990-164103 (JP02164103 Heisei) 19900625

04/10/2002

Serial No.:09/852,847

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1216, Vol. 16, No. 263, P. 90 (19920615)

AB PURPOSE: To conduct high-density packaging by forming pads for repair around package substrates, on which semiconductor **chips** are loaded, loading the semiconductor **chips** on the package substrates and loading a plurality of module units composed of **chips** and substrates on a **wiring** board.

CONSTITUTION: A **chip** 2 is loaded to the upper section of a package substrate 1, and a plurality of pads 4 for repair are formed around the **chip** 2 at proper intervals. These module units 3 are loaded to the upper section of a **wiring** board 5 by **bump electrodes** 6, and a plurality of leads are provided drooping in the downward direction from the rear of the **wiring** board 5. These leads 7 are **mounted** into the through-holes of the printed **circuit** board 8 of the lower section of the **wiring** board 5. The leads 7 are **connected electrically** to the **bump electrodes** 6 by the internal wirings of the **wiring** board 5, and further **connected electrically** to the internal wirings of the **chips** 2 through the internal wirings of the package substrates 1. Accordingly, since the pads for repair are formed onto the package substrates in the module units, high-density **mounting** is enabled, repair operation is facilitated, and defective **chips** can be utilized.

L34 ANSWER 57 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1991-169062 JAPIO

TI SEMICONDUCTOR DEVICE

IN GOTO SEIJI

PA NEC KYUSHU LTD, JP (CO 423996)

PI JP 03169062 A 19910722 Heisei

AI JP1989-310161 (JP01310161 Heisei) 19891128

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1123, Vol. 15, No. 4, P. 150 (19911017)

AB PURPOSE: To reduce a package occupation area of a semiconductor device on a **circuit** board and to improve integration of a **circuit** board by **stacking** semiconductor **chips** solidly.

CONSTITUTION: A first semiconductor **chip** 1 is **mounted** on an island 5. An inner lead 6 provided on the periphery of the island 5 and a pad **electrode** 7 provided on the peripheral **edge** part of the semiconductor **chip** 1 are connected by a thin metal **wire** 4. Then, a second semiconductor **chip** 2 is **mounted** which has a bump 3 corresponding to a pad **electrode** 8 provided inside the pad **electrode** 7; the pad **electrode** 8 and the bump 3 are bonded by pressure; and the semiconductor **chip** 1 and the semiconductor **chip** 2 are **electrically connected**. Thereby, it is possible to reduce a package occupation area of a semiconductor device on a **circuit** board and to improve integration of a **circuit** board.

L34 ANSWER 58 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1991-049246 JAPIO

TI SEMICONDUCTOR **INTEGRATED CIRCUIT** DEVICE

IN YOSHIDA IKUO

PA HITACHI LTD, JP (CO 000510)

PI JP 03049246 A 19910304 Heisei

AI JP1989-184367 (JP01184367 Heisei) 19890717

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.

1067, Vol. 15, No. 187, P. 143 (19910514)

AB PURPOSE: To prevent fluctuation etc., in electrical characteristics due to contaminant by a method wherein an element forming surface of a semiconductor **chip mounted** on an Si substrate via a CCB bump is sealed airtight by a sealing part extended on the outer periphery of the **chip**.

CONSTITUTION: A device **hole 2** is drilled at the center of a film carrier 2. An Si **wiring** substrate 4a is placed inside the **hole 2**. At the center of this substrate 4a, a semiconductor **chip 8** with an **integrated circuit** formed is **mounted** via a CCB bump with an element forming surface facing downward. The element forming surface of the **chip 8** is sealed airtight by a sealing part 10 extended along the outer periphery of the **chip 8**. The bump 9 is **electrically connected** to an **electrode** via a bed metal 6c formed on the substrate 4a. This **electrode** is **electrically connected** to a **bump electrode 7** formed on the outer periphery of the substrate 4a. In addition, this **electrode 7** is bonded to an inner lead 3a of a lead 3. Thus elements and **wiring** can be protected against contaminants such as moisture.

L34 ANSWER 59 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1986-089657 JAPIO

TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

IN KONDO SHUJI

PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)

PI JP 61089657 A 19860507 Showa

AI JP1984-211101 (JP59211101 Showa) 19841008

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 435, Vol. 1, No. 263, P. 132 (19860909)

AB PURPOSE: To **mount** in high density by a flip-**chip** method or tape-carrier method useful for reducing a **mounting** size by providing a main **chip** provided at a function element region at the center of the main surface, an **electrode bump** for connecting an external conductor, a barrier bump provided on the main surface of the **chip**, and a hermetically sealed sub **chip**.

CONSTITUTION: Function element regions 9, 10 as semiconductor devices are provided on a main **chip** substrate 7 and a sub **chip** substrate 8, mutually connected **electrode** groups 11, 12 are provided on the outer periphery, and the regions 9, 10 are electrically coupled by metal **wiring** pattern as required. External conductor connecting **electrode** pad group 13 is formed near the peripheral **edge** of the main **chip 7**, and **electrically connected** with the **wiring** pattern 15 under a protective film layer 14 with the group 11. The electromechanical coupling between the **chips 7** and 9 having the basic structures used a flip-**chip** type. The **chips 7** and 9 are all formed in the same steps as the normal semiconductor device manufacturing **wafer** process, and the process of forming the bump is then added.

L34 ANSWER 60 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1985-198758 JAPIO

TI SEMICONDUCTOR DEVICE

IN EMOTO YOSHIAKI; OTSUKA KANJI; KOBAYASHI TSUNEO

PA HITACHI LTD, JP (CO 000510)

PI JP 60198758 A 19851008 Showa

AI JP1984-54208 (JP59054208 Showa) 19840323

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.

382, Vol. 1, No. 42, P. 90 (19860219)

AB PURPOSE: To accomplish efficient heat dissipation by a method wherein a multilayer **wiring** layer is formed over one surface of a substrate having a high thermal conductivity and almost the same coefficient of thermal expansion as that of a **chip** provided thereon, and a **chip** is **mounted** on the opposite surface, both of which are then connected with through **hole** wirings.

CONSTITUTION: A substrate 1 of silicon carbide formed by hot press and containing 0.1-3.5wt% of beryllium of high thermal conductivity is provided with the through **hole** wirings 2 penetrating through this substrate in the thickness direction thereof. The through **hole wiring** 2 **electrically connects** the multilayer **wiring** layer 3 formed on the back of the substrate 1 to the **chip** 8 **mounted** on the front of the substrate 1. Signal wirings 4 and power source wirings 5 are connected to installation **electrodes** 6 to install the **chip** 8 respectively via through **hole wiring** 2. Many **chips** 8 are installed to the installation **electrodes** 6 with connection **bumps** 9. A forced cooling member 10 is provided so as to surround the side surface of the substrate 1.

L34 ANSWER 61 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1985-148151 JAPIO

TI SEMICONDUCTOR DEVICE

IN INABA TORU

PA HITACHI LTD, JP (CO 000510)

PI JP 60148151 A 19850805 Showa

AI JP1984-3425 (JP59003425 Showa) 19840113

SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 365, Vol. 9, No. 3151, P. 63 (19851211)

AB PURPOSE: To simplify the package constitution of a semiconductor device by a method wherein the connection of external connection terminals to a semiconductor **chip** is performed using a supporting substrate provided with a butt contact part.

CONSTITUTION: Aluminum **electrodes** 5 are provided on the surface of a semiconductor **chip** 1, wherein semiconductor elements 4 have been formed, and at the same time, a silver **bump electrode** 6 is each formed on parts of the aluminum **electrodes** 5 as a pad. Meanwhile, a supporting substrate 2 is provided for leading out the above-mentioned **electrodes** 6 to external terminals. A **wiring** layer 8, which comes in contact with the above-mentioned **electrodes** 6, external connection terminals 9 are provided on the supporting substrate 2. The terminals 9 are both constituted by forming a metallized **wiring** in each semicircular **groove** 10 formed on both sides of the supporting substrate 2. These **grooves** 10 receive connection terminals erected on the substrate 2 therein when this semiconductor device is **mounted** on a printed substrate and make to **electrically connect** the connection terminals and the terminals 9. Sealing mediums 11 and 12 are formed on the periphery of the main surface of the **chip** 1, where the **chip** 1 is opposing to the supporting substrate 2, in such a way as to encircle the interior of the **chip** 1.

L34 ANSWER 62 OF 62 JAPIO COPYRIGHT 2002 JPO

AN 1984-126658 JAPIO

TI HYBRID INTEGRATED CIRCUIT

IN HAYASHI TETSUO; OSATO MASATOSHI

04/10/2002

Serial No.:09/852,847

PA NEC CORP, JP (CO 000423)
PI JP 59126658 A 19840721 Showa
AI JP1983-1851 (JP58001851 Showa) 19830110
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 279, Vol. 8, No. 25, P. 93 (19841116)
AB PURPOSE: To previously perform the test for evaluating IC chips and facilitate the exchange of defective IC chips after mounting by adhesion-fixing electrode patterns of the first and second substrate after the first substrate loaded with an IC chip is combined with the second substrate wherein it can be fitted.
CONSTITUTION: After fusing the IC chip 3 to the first substrate 7 by means of solder, the bonding pads of the IC chip 3 are connected to the electrode wiring pattern 8 by means of bonding wires 4. The test for the IC chip 3 is performed at this step.
Non-defectives whose reliability is ensured are opposed to each other so that the surface for loading the IC chip 3 of the first substrate 7 contact the surface whereon the electrode wiring pattern 2 of the second substrate 2 is laid, and so that the IC chip 3 may come in the right position of a relief hole 9, thus electrically connecting the corresponding electrode wiring patterns 8 and 2 of both the substrates by a method such as soldering. If there are IC chips judged as defective in the test for the entire body after completing a hybrid IC, the first substrate thereof is removed by fusing again the solder and then exchanged.

FILE 'INSPEC, HCAPLUS' ENTERED

L1 1107371 S (TRENCH## OR HOLE OR GROOVE OR CHANNEL OR EDGE
OR FLUSH OR RIDGE)
L2 17178 S (SOLDER OR SOLDERING OR SOLDERED OR BRAZ? OR
POLYMER?)(2N)(BALL OR BALLS OR PADS OR PAD OR SPHERE OR COLUMN
OR COLUMNS OR POST OR POSTS OR SPHERE OR SPHERES) OR ((BALL OR
PLATE OR BUMP)(3N)(ELECTRODE OR ELECTRODES)) OR (STUD OR
INTERPOSER)(3N)(BUMP OR BUMPS)
L3 929359 SEA ABB=ON PLU=ON IC OR ICS OR ((INTEGRATED OR
LOGIC)(W)(CIRCUIT)) OR (MICRO)(W)(CIRCUIT OR CHIP OR ELECTRONIC?)
OR CHIP OR MICROCIRCUIT OR DIE OR DICE OR WAFER OR
MICROELECTRONIC? OR CIRCUIT
L4 3283181 S CONNECT? OR JOIN### OR COMBINE OR CONJOIN? OR
CONJUGAT? OR CONSOLIDATE OR COUPL? OR LINK### OR UNIF### OR
UNIT#### OR YOKE
L5 2630959 SWIR### OR LIN###
L6 284761 S STACK### OR MOUNT? OR PILE OR PILED OR MOUND?
L7 3649 S L3 AND L2
L8 847 S L7 AND L5
L9 136 S L8 AND RESIN
L10 33 S L9 AND L1
L11 33 DUP REMOVE L10 (0 DUPLICATES REMOVED)

L12 290 S L8 AND L6
L13 186 S L12 AND L4
L14 14353 S (ELECTRICALLY)(2N)(CONNECT? OR JOIN? OR
INTERCONNECT)
L15 25 S L13 AND L14
L16 25 DUP REMOVE L15 (0 DUPLICATES REMOVED)
L17 21 S L16 NOT L11

L18 22 S L9 AND L14
L19 6 S L18 NOT (L11 OR L17)

L20 1704 S L7 AND L4
541 S L20 AND ELECTRODE
L21 467 S L20 AND L5
L22 186 S L21 AND L6
L23 36 S L22 AND RESIN
L24 15 S L23 NOT (L10 OR L15 OR L18 OR L19)
D BIB AB 1-15

04/10/2002

Serial No.:09/852,847

L11 ANSWER 1 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:90396 HCAPLUS

DN 136:143730

TI Vertically integrated **chip** on **chip** circuit
stack

IN Vindasius, Alfons; Robinson, Marc E.

PA Vertical Circuits, Inc., USA

SO PCT Int. Appl., 40 pp.

CODEN: PIXXD2

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2002009181	A1	20020131	WO 2001-US23018	20010720
	W:	AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM			
	RW:	GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG			

PRAI US 2000-620011 A 20000720

AB A vertically integrated **chip** on **chip** circuit stack provides a vertically integrated stack of **die** which includes two or more **integrated circuit die**, with the faces (circuitry) of the resp. **die** surface up. The **die** are desirably of identical size, (length, and width). The **die** have elec. contacts at the **edges** of the top surface (face surface) and the bottom surface of each **die** is coated with an epoxy adhesive or glue where the adhesive is an elec. insulator. A spacer is between each **integrated circuit die** and sufficient thickness to allow write bond loops to be formed above such that the **wires** connected to the lower **die** do not touch the bottom surface of the **die** above. Elec. conducting **wires** are bonded to selected elec. contacts on each **integrated circuit die**. The conducting **wires** can be, for example, gold **wires**, or aluminum **wires**. The 2nd end of the conducting **wires** are bonded to elec. conductors on a substrate which has elec. conductors. The elec. conductors on the top surface of the substrate are elec. connected to **solder balls** on a bottom surface of substrate. The stack and substrate can be molded in plastic, non conducting epoxy **resin**, other suitable molding compd. or encapsulant.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 2 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:202559 HCAPLUS

TI Method of fabricating an electronic component and apparatus used therefor

IN Takehara, Masataka; Nakagawa, Osamu

PA Towa Corporation, Japan

SO U.S., 9 pp.

CODEN: USXXAM

DT Patent

LA English

04/10/2002

Serial No.:09/852,847

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6358776	B1	20020319	US 2000-705239	20001102
PRAI	JP 1999-316209	A	19991108		

AB The present invention provides a method of fabricating an electronic component, using a tool for pressing a **chip** against a substrate and heating the same, connecting a **chip** electrode and a substrate **electrode** together via a **bump**, placing the substrate in alignment with a **die** alignment plane for an upper **die** and a lower **die**, clamping the upper **die** and the lower **die** to form a cavity and exhausting the cavity via an exhaust **hole** to evacuate the same, and injecting melted **resin** into the cavity and curing the melted **resin** to provide sealing **resin**. Then, in a predetermined ambient at a predetermined temperature the substrate is pressed against a test board and a predetermined electrical signal is applied from the test board via an external electrode to the **chip** to test an operation of an electronic component configured on a unit region of the substrate and the **chip**. Thereafter, cutting along a virtual **line** completes the electronic component. Thus, a plurality of **chips** can be **resin**-sealed collectively with high precision and a plurality of electronic components can be burnt in. As a result, in mounting the **chip** to the substrate, sealing the same with **resin** and burning in the same to provide an electronic component, the electronic component can be efficiently fabricated, with the sealing **resin** having a dimension with high precision.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 3 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:256776 HCAPLUS
TI A method of manufacturing a semiconductor device
IN Fujisawa, Atsushi
PA Japan
SO U.S. Pat. Appl. Publ., 30 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002039811	A1	20020404	US 2001-934651	20010823
PRAI	JP 2000-298941	A	20000929		

AB A semiconductor device comprising: a tape substrates 2for supporting a semiconductor **chip** 1;wires 4for connecting the pads of the semiconductor **chip** 1and the connection terminals of the tape substrates 2;a sealing portion formed on the **chip** supporting face 2aof the tape substrates 2for **resin**-sealing the semiconductor **chip** 1;and a plurality of **solder balls** disposed on the back face 2bof the tape substrates 2.After a block molding operation for **resin**-molding a plurality of device areas altogether, the semiconductor device is diced and individualized. By performing the block-molding operation using a molding tool having protrusions 13con a cavity forming face 13a,grooves 8aare formed in the surface of a block-molded portion 8when this portion 8is formed. Therefore, the tensile deformation of the surface of the block-molded portion 8at the setting/shrinking time of a molding **resin** 14is relaxed by the **grooves** 8ato reduce the warpage of the

04/10/2002

Serial No.:09/852,847

block-molded portion 8after the resin was set.

L11 ANSWER 4 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:103603 HCAPLUS
TI Semiconductor device and manufacturing method thereof
IN Shintani, Susumu
PA Japan
SO U.S. Pat. Appl. Publ.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002016022	A1	20020207	US 2001-886035	20010622
PRAI	JP 2000-194780	A	20000628		

AB A semiconductor device is arranged such that a semiconductor chip having electrodes is flip chip mounted on printed substrate pads on a printed wiring substrate by a bump formed on each electrode. The semiconductor chip and the printed wiring substrate are fixed with a thermo-setting resin. A penetration hole is formed within an area where the printed substrate pad contacts each gold bump, and the gold bump has a joint section also on a side face of the penetration hole of the printed substrate pad. With this structure, the semiconductor device has a secure electrical connection between the bump and the metal pattern.

L11 ANSWER 5 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:830934 HCAPLUS
DN 135:365520
TI Highly reliable ball-grid-array package construction under thermal stress of semiconductor device
IN Baba, Shinji
PA Mitsubishi Denki Kabushiki Kaisha, Japan
SO U.S., 12 pp., Cont.-in-part of U.S. Ser. No. 61,022, abandoned.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6317333	B1	20011113	US 1999-427583	19991027
PRAI	JP 1997-231927	A	19970828		
	US 1998-61022	B2	19980416		

AB A semiconductor device includes a ball grid array substrate including an upper insulating layer of laminated insulating layers, an intermediate insulating layer, and a lower insulating layer of laminated insulating layers; lines on each top surface of the insulating layers included in the upper insulating layer, the intermediate insulating layer, and the lower insulating layer, resp.; and a semiconductor chip having electrodes connected to the lines, the semiconductor chip being connected with solder balls through via holes in each of the insulating layers, the solder balls being located on an outermost surface of the lower insulating layer.

RE.CNT 34 THERE ARE 34 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

04/10/2002

Serial No.:09/852,847

=> D BIB AB 6-33

L11 ANSWER 6 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:278058 HCAPLUS

DN 134:274568

TI Mold-BGA-type semiconductor device and method for making the same

IN Kimura, Naoto

PA NEC Corporation, Japan

SO U.S., 7 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6218728	B1	20010417	US 1998-179154	19981026
PRAI	JP 1997-295305	A	19971028		

AB Disclosed is a mold-BGA-type semiconductor device which has: a semiconductor **chip** which includes insulating **resin** film formed on at least a part of the surface of the semiconductor **chip** except a pad; a conductive layer formed in a region on the insulating **resin** film, the region including at least part corresponding to a position where a **solder ball** is mounted; a 1st metal thin **wire** which is **wire**-bonded between the pad and the conductive layer; a 2nd metal thin **wire** which is **wire**-bonded on the conductive layer; **resin** part which seals the semiconductor **chip**, the **resin** part including a **hole** to expose part of the 2nd metal thin **wire**; and a **solder ball** which is mounted on the **hole**.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 7 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:523780 HCAPLUS

DN 135:130695

TI Printed **wiring** board for extremely thin BGA semiconductor plastic package

IN Take, Morio; Ikekuchi, Nobuyuki; Yoshida, Taro

PA Mitsubishi Gas Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001196492	A2	20010719	JP 2000-2232	20000111

AB The title **wiring** board comprises an one-side Cu-clad board of an insulator layer (40 - 150 .mu.m) from .gtoreq.1 glass cloth having an air permeability .ltoreq. 25 cm3/cm2.bul.s, **wire**-bonding terminals formed at the bottoms of **holes** opened in the board from the **resin** side of the board to reach the Cu foil, **solder ball** bonding **pads** on the Cu foil, and a Cu foil **circuit** for connecting the **wire**-bonding terminals and bonding pads.

L11 ANSWER 8 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:299930 HCAPLUS

04/10/2002

Serial No.:09/852,847

TI Semiconductor device. [Machine Translation].
IN Osono, Takeaki
PA Mitsui High-Tec, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001118954	A2	20010427	JP 1999-298318	19991020

AB [Machine Translation of Descriptors]. As for theme of this invention, the laminate the semiconductor **chip** of the optional quantity is possible without accompanying the enlargement of plane surface size to do, and also, there are times when the possible semiconductor device of the thing which achieves also shortening the lead time is offered. As the semiconductor device 1 which relates to this invention the baseplate one side of 10 where on one hand **wiring** pattern 11 was formed to the surface and said baseplate 10 the loading being done on the surface, **wiring** pattern 11 has with the semiconductor **chip** 2 which, is connected electrically at least semiconductor **chip** the **resin** seals the terminal area of 2 and **wiring** pattern and 11 becomes, projects **edge** 10 E of baseplate 10 to package (**resin** seal section) 3 outside, the **solder ball** 4 which **wiring** pattern 11 is connected to the **edge** 10 E of baseplate 10 is provided.

L11 ANSWER 9 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:265153 HCAPLUS
DN 134:304090
TI Printed **wiring** board for extremely thin BGA-type semiconductor plastic package
IN Takashi, Morio; Ikekuchi, Nobuyuki; Shimizu, Kenichi
PA Mitsubishi Gas Chemical Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001102491	A2	20010413	JP 1999-273130	19990927

AB The title **wiring** board comprises a glass-cloth one-side Cu-clad laminated board having an insulator-layer thickness 40 - 150 .mu.m and **ball-soldering** via **holes** reaching the backside of the Cu foil from the **resin** side of the board, terminals for semiconductor **chip** bonding on the Cu foil, and **pads** for **solder-ball** bonding at the backside of the board. Specifically, the glass cloth may comprises a glass woven fabric having a thickness 50 .+- . 10 .mu.m, wt. 35 - 60 g/m2, and air permeability .ltoreq. 25 cm3/cm2.bul.s. The board has an improved Shore hardness.

L11 ANSWER 10 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:46979 HCAPLUS
TI Semiconductor device and its production method. [Machine Translation].
IN Terashima, Kazuhiko
PA Citizen Watch Co., Ltd., Japan
SO Jpn. Kokai Tokkyo Koho, 11 pp.
CODEN: JKXXAF

04/10/2002

Serial No.:09/852,847

DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001015647	A2	20010119	JP 2000-122859	20000424
	US 6329228	B1	20011211	US 2000-559311	20000427
PRAI	JP 1999-122659	A	19990428		

AB [Machine Translation of Descriptors]. The margin of the **resin** seal body that tries does not break easily, crack occurs in the **resin** seal body, an other electronic component and, with that fragment kind of the fact that function of the part conveyor is inhibited is prevented. Each baseplate electrode possesses the **resin** seal body 8 which the chart surface whole surface the covering is done in order to protect 3 which is connected to the chart surface of **wiring** baseplate 1, electrically semiconductor **integrated circuit tip/chip** with each electrode and the respective connected **wire** 7 of 2 and that semiconductor **integrated circuit tip/chip** 2 and semiconductor **integrated circuit tip/chip** 2, on the and others aspect of **wiring** baseplate 1, padding electrode possesses 9 in order to connect with the motherboard and **solder ball** terminal 10, baseplate **electrode** 3 of the chart surface of **wiring** baseplate 1 questions and others possesses the through **hole** 11 in order to connect with the padding electrode 9 of the surface electrically the PBGA structure which Semiconductor device 12 is, margin 8 A of **resin** seal body 8 has formed curved surface form.

L11 ANSWER 11 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:677180 HCAPLUS

DN 135:219865

TI Flip **chip** type semiconductor device with **wiring** pattern pitch less than 10 .mu.m and low-cost method for manufacturing the same

IN Honda, Hirokazu

PA Nec Corporation, Japan

SO U.S. Pat. Appl. Publ., 25 pp.

CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001020739	A1	20010913	US 2001-801901	20010309
PRAI	JP 2000-65792	A	20000309		

AB A multilayer **wiring** structure is formed on a flat metal plate and then an entire surface of the metal plate is etched away to thereby leave only a multilayer **wiring** layer. An insulating substrate having through **hole** sections is bonded to the multilayer **wiring** layer, a conductive bonding agent is embedded into the through **hole** section, a semiconductor **chip** is mounted and a **solder ball** is coupled.

L11 ANSWER 12 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:814774 HCAPLUS

DN 133:358177

TI Method for manufacturing a printed **circuit** board with integrated heat sink for semiconductor package

IN Juskey, Frank J.; McMillan, John R.; Huemoeller, Ronald P.

04/10/2002

Serial No.:09/852,847

PA Amkor Technology, Inc., USA
 SO PCT Int. Appl., 24 pp.
 CODEN: PIXXD2
 DT Patent
 LA English
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2000069239	A1	20001116	WO 2000-US13041	20000511
	W: CA, JP, KR, SG				
	RW: AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE				
	US 6337228	B1	20020108	US 1999-310660	19990512
PRAI	US 1999-310660	A	19990512		
AB	A low-cost printed circuit board (10) for a semiconductor package having the footprint of a ball grid array package has an integral heat sink (20), or slug, for the mounting of one or more semiconductor chips , capable of efficiently conducting away at least five watts from the package in typical applications. It is made by forming an opening (16) through a sheet, or substrate (14), of B-stage epoxy/fiberglass composite, or pre-preg, then inserting a slug (20) of a thermally conductive material having the same size and shape as the opening into the opening. The slug-contg. composite is sandwiched between two thin layers (30) of a conductive metal, preferably Cu, and the resulting sandwich (10) is simultaneously pressed and heated between the platen (12) of a heated press. The heat and pressure forces the resin to the surface of the composite (10) and into the space between the slug (20) and the walls of the composite, where it solidifies, bonding the edges of the slug (20) to the substrate (14) within the opening and adhering the conductive layers (30) to the upper and lower surfaces of the substrate (14). The resulting laminate (10) can thereafter be processed as a convention printed circuit board to incorporate conventional circuit board features, e.g., circuit traces, wire bonding pads , solder ball mounting lands, and via holes .				

RE.CNT 4 THERE ARE 4 CITED REFERENCES AVAILABLE FOR THIS RECORD
 ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 13 OF 33 HCAPLUS COPYRIGHT 2002 ACS
 AN 2000:907226 HCAPLUS
 TI BGA type semiconductor device. [Machine Translation].
 IN Yamamoto, Kazuhiro; Aida, Kazuhiro; Kawanobe, Naoshi
 PA Hitachi Cable, Ltd., Japan
 SO Jpn. Kokai Tokkyo Koho, 4 pp.
 CODEN: JKXXAF

DT Patent
 LA Japanese
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000357761	A2	20001226	JP 1999-170758	19990617
AB	[Machine Translation of Descriptors]. The insulating-film, the temp. stress absorption effective material which possesses the adhesive property, exfoliation between the layer of the IC tip/ chip is prevented, the BGA type semiconductor device in order at the same time to prevent the damage of the IC tip/ chip corner section is offered. Possesses of the temp. stress absorption effective material and the solder ball for connection outside is connected to the aforementioned plural lands of the				

aforementioned insulating-film and the connected part of aforementioned plural inner leads/reads and the aforementioned plural bonding pads which possess the IC tip/chip and the bonding hole, with this bonding hole with aforementioned plural inner leads/reads with the specified wiring pattern adhesion the plural lands in order to connect these to external circuit all over of the wiring film, and the aforementioned insulating-film which consist of the insulating-film which the formation is done in the 1st aspect, possess the adhesive property in the aforementioned semiconductor chip adhesion in the 2nd aspect the bonding hole which In order the aforementioned seal resin to be connected, with the similar seal resin applying 2 sides where the particular semiconductor device opposes at least in the BGA semiconductor device which has the seal resin which seals, with the sep. resin, offers the BGA type semiconductor device which designates that is constituted as feature.

L11 ANSWER 14 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:823362 HCAPLUS

DN 134:12356

TI Manufacture of metal core plates for printed circuit boards

IN Ikekuchi, Nobuyuki; Kobayashi, Toshihiko

PA Mitsubishi Gas Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000323836	A2	20001124	JP 1999-133333	19990513
AB	The title manufg. involves opening clearance holes and/or slits to a metal core plate, pressing the plate by a jig to give the plate conical plateau projections in the area for mounting semiconductor chips, and coating a thermosetting polymer insulator over the projections on the both sides of the plate. A signal transmission circuit provided on one side of the plate substrate and other circuit provided on the other are insulated from the metal core plate and connected to the semiconductor chips by wire -bonding or flip-chip bonding. The thermosetting polymer insulator may be made from polyfunctional cyanate ester polymers or cyanate ester prepolymers. The metal core plate may be made of Cu or Cu-alloy. The materials give the circuit boards increased adhesion to solder balls, decreased moisture absorption, and improved pop-corn effects in thermal resistance.				

L11 ANSWER 15 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:747539 HCAPLUS

TI Semiconductor device. [Machine Translation].

IN Ito, Osamu; Goto, Makoto

PA Hitachi Cable, Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000299410	A2	20001024	JP 1999-106490	19990414

04/10/2002

Serial No.:09/852,847

AB [Machine Translation of Descriptors]. Is superior in heat cycle tolerance by designating the covering length of the seal **resin** in the side of the semiconductor **chip** as fixed ones always, offers the profitable semiconductor device even costwise. In the insulating-film through temperature stress relief layer 3 1 which **wiring** layer 2 of the specified pattern the formation is done and **wiring** layer 2 on the aspect of one side, the **solder ball** in **electrode** 10 of 7 which connect to the specified place of **wiring** layer 2 the semiconductor **chip** through 3 which the loading is done, and penetration **hole** 8 on the other aspect of insulating-film 1 arrange in array condition and semiconductor **chip** 4 lead/read 9 of the **wiring** layer 2 which the bonding is done and lead/read in the semiconductor device which is formed from the seal **resin** 11 which the formation is done around 9 and **electrode** 10, on the side of semiconductor **chip** 4 **resin** stopping section 5 The formation it does, extends seal **resin** 11 up to this **resin** stopping section 5 and the covering it does the specified area 6 of semiconductor **chip** 4 with seal **resin** 11 by the formation doing.

L11 ANSWER 16 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:534563 HCAPLUS

DN 133:158603

TI Manufacture of **resin**-sealed semiconductor devices

IN Oka, Takahiro

PA Oki Electric Industry Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 9 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000216178	A2	20000804	JP 1999-12239	19990120
	US 6174751	B1	20010116	US 2000-484900	20000118
PRAI	JP 1999-12239	A	19990120		

AB **Bump electrodes** of semiconductor devices on **wafers** and inner bads on substrates are matched, and elec. connected, the gaps between the **wafers** and substrates are filled with **resins** injected from injection **holes**, the **resins** are hardened, and the substrates and **wafers** are cut along cut **lines** as well as scribe **lines**.

L11 ANSWER 17 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:418652 HCAPLUS

TI Semiconductor device. [Machine Translation].

IN Iijima, Maki; Ueno, Kiyoharu; Sakumoto, Noriya; [NAME NOT TRANSLATED], Hiroshi

PA Fujitsu Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 8 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000174162	A2	20000623	JP 1998-347418	19981207

AB [Machine Translation of Descriptors]. This invention designates that densification is made possible at low cost in regard to the semiconductor

device which uses flip tip/**chip** technology, as theme. The semiconductor component 12 which makes the constitution which the face down bonding is done and the surrounding terminal area 17 A - 17 B where external connected terminal such as **solder ball** is connected and inside the bump 14 which is provided in semiconductor component 12 is connected the formation doing the **wiring** layer 16 A - 16 C which terminal area 18 A - 18 C ingredient preparation is done on **resin** tape 15 A - 15 C, the plural layer (with this execution example 3 layers) laminates doing the baseplate layer 20 A - 20 C which, becomes providing with the laminate baseplate 13 A which, becomes it becomes. In addition, as bump 14 and the projection electrode 21 which the bonding is done and 22 the formation is done respectively on the inside terminal area 18 A - 18 C of each baseplate layer 20 A - 20 C which forms laminate baseplate 13 A, in order this each projection electrode for the point of 21 and 22 to become **flush** mutually, constitutes.

L11 ANSWER 18 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:362983 HCAPLUS

DN 133:11859

TI Printed **circuit** board for plastic-packaged semiconductor device

IN Oka, Morio; Ikeguchi, Nobuyuki; Kobayashi, Toshihiko

PA Mitsubishi Gas Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000150714	A2	20000530	JP 1998-333452	19981109
AB	The circuit board involves an inserted metal plate, with the similar size as the board, placed at the middle of the thickness and the metal plate has bumps, which are elec. connected to a Cu layer formed on the surface of semiconductor chips on the board and another Cu layer on the opposite side of the board having heat-releasing solder ball pads . The semiconductor chips are bonded on the board by a heat-conductive adhesive, the inserted metal plate is elec. insulated with elec. circuits on the surface of the board by intermediate thermosetting resin layers, the semiconductor chips and the circuits are connected by wire bonding, elec. conductors involved in the boards are connected by through holes , and the semiconductor chips , wires , and bonding pads are packaged with a plastic. So-called popcorn phenomena, i.e., blister under heat in mounting the board on mother board, etc., is prevented.				

L11 ANSWER 19 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:88498 HCAPLUS

DN 132:145353

TI Glassy carbon **electrode plate** for plasma etching

IN Hironaka, Shintaro; Kamata, Atsushi; Suzuki, Takayuki

PA Hitachi Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 4 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

04/10/2002

Serial No.:09/852,847

PI JP 2000040689 A2 20000208 JP 1998-208078 19980723
AB The **electrode plate** is made of a glassy carbon substrate having pierced small **holes** in the center part and the max. center line av. roughness Ra (JIS B 0601) measured at .gtoreq.5 points on the surface consumed in plasma etching is 0.008-0.09 .mu.m. Contamination of the **wafer** with carbon dropped from the electrode is prevented. in the plasma etching in semiconductor device fabrication.

L11 ANSWER 20 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:767905 HCAPLUS

TI Method of producing a ball grid array type printed **wiring** board having excellent heat diffusibility and printed **wiring** board

IN Kimbara, Hidenori; Ikeguchi, Nobuyuki; Komatsu, Katsuji

PA Mitsubishi Gas Chemical Company, Inc., Japan

SO Eur. Pat. Appl.

CODEN: EPXXDW

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	EP 1049151	A2	20001102	EP 2000-303592	20000428
	R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO				
	JP 2000315749	A2	20001114	JP 1999-125051	19990430
	JP 2000315750	A2	20001114	JP 1999-125055	19990430
	JP 2001007533	A2	20010112	JP 1999-174549	19990621
PRAI	JP 1999-125051	A	19990430		
	JP 1999-125055	A	19990430		
	JP 1999-174549	A	19990621		
AB	A method of producing a printed wiring board for a ball grid array type semiconductor plastic package which has excellent heat diffusibility and causes no popcorn phenomenon, and a metal-plate-inserted printed wiring board having wire bonding pads formed at two levels, for use in the ball grid array type semiconductor plastic package, the printed wiring board having a structure in which the metal plate is placed in a region located as part of the thickness direction of a printed wiring board, the metal plate has a flat region in one surface, a plurality of metal protrusions having the form of frustum of a cone each are formed in the other surface of the metal plate so as to be connected to a copper foil forming a reverse surface, the metal plate has a size nearly equiv. to the size of the printed wiring board. A semiconductor is fixed on the flat region located at a level lower than the level of a signal propagation circuit and circumferential bonding pads of two levels on one surface of the printed wiring board, the metal plate and a signal propagation circuit conductor on the front surface of the printed wiring board are insulated from each other with a thermosetting resin compn., the signal propagation circuit conductor and the semiconductor chip are connected through the bonding pads of two levels by wire bonding, and at least the signal propagation circuit conductor on the front surface of the printed wiring board and a circuit conductor formed on an opposite surface of the printed wiring board or circuit conductor pads formed on the opposite surface of the printed wiring board for connecting the package to an outside with solder balls are connected with a through hole conductor insulated from the metal plate with a resin				

04/10/2002

Serial No.:09/852,847

compn.

L11 ANSWER 21 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 2002:101381 HCAPLUS
DN 136:127463
TI Stack package for a semiconductor device
IN Cho, Sun Jin
PA Hyundai Electronics Ind. Co., Ltd., S. Korea
SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
CODEN: KRXXA7
DT Patent
LA Korean
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2000020479	A	20000415	KR 1998-39092	19980921
AB	A package is provided which makes stable elec. connection and has a low manufg. price by using a substrate on which circuits are formed instead of lead frame. On both sides of a plastic substrate, upper and lower metal interconnecting layers are attached. Lower thermosetting resin having slot in its mid portion is attached to bottom surface of the lower metal interconnecting layer. On the bottom surface of the lower thermosetting resin , metal interconnecting layer is attached. Via holes are formed on the substrate. Both inner wall of the via holes and top and bottom metal interconnects are coated by conductive metal to elec. connect resp. metal interconnecting layer. An upper semiconductor chip is attached to middle top part of upper thermosetting resin between metal interconnecting layers whereas a lower semiconductor chip is attached to lower part of that by a bonding agent, these chips being connected to each metal interconnecting layer by a metal wire . By sealing agent, all of the top part are molded and the portion between the metal interconnecting layer is also molded. A solder ball mounted to the substrate is attached to bottom surface of lowest metal interconnecting layer exposed to downwards from the ball agent.				

L11 ANSWER 22 OF 33 INSPEC COPYRIGHT 2002 IEE
AN 2002:7167748 INSPEC DN B2002-03-0170J-016
TI New flip-**chip** bonding technology NSD (non conductive film **stud-bump** direct interconnection) method using **resin** encapsulation sheet - examination of joint reliability on ALIVH substrate.
AU Nishida, K.; Nishikawa, H.; Shimizu, K.; Otani, H. (Circuit Manuf. Process Technol. Lab., Matsushita Electr. Ind. Co. Ltd., Osaka, Japan); Koguchi, H.
SO Proceedings 2000 International Symposium on Microelectronics (SPIE Vol.4339)
Reston, VA, USA: IMAPS - Int. Microelectron. & Packaging Soc, 2000.
p.287-92 of xx+886 pp. 3 refs.
Conference: Boston, MA, USA, 18-20 Sept 2000
Sponsor(s): SPIE; IMAPS - Int. Microelectron. & Packaging Soc
ISBN: 0-930815-62-9
DT Conference Article
TC Practical
CY United States
LA English
AB This paper describes a newly developed flip-**chip** process called the NSD (Non-conductive Film **Stud-bump** Direct Interconnection) method. In the first step, an encapsulation sheet is

attached to the substrate by heat compression. **Stud-bumps** are formed on an **IC chip** by means of conventional **wire-bonding** technology. The **IC chip** with bumps is then attached to the substrate. In the final process, the encapsulation sheet is heated and compressed using a heated tool, during which the **stud-bumps** make contact with the electrodes on the substrate to form electrical interconnections and follows to the substrate warp. When the encapsulation sheet cools, compression force is generated between the **IC chip** and substrate, which helps to maintain the interconnections. Highly reliable interconnections were obtained by optimizing the properties of the **resin** encapsulation sheet using the FEM. This article reports on the relationship between the properties of the encapsulation sheet and reliability when bare **IC chips** are attached using the NSD method onto an ALIVH (Any Layer Inner Via **Hole**) substrate, which utilizes unique epoxy-impregnated aramid non-woven cloth.

L11 ANSWER 23 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 1999:498846 HCAPLUS

DN 131:178570

TI Peripheral lower heat-release semiconductor plastic package

IN Take, Morio; Ikeguchi, Nobuyuki; Yamane, Kozo

PA Mitsubishi Gas Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11220063	A2	19990810	JP 1998-34233	19980130

AB A semiconductor **chip** is directly mounted on a printed **circuit** board and the **chip** is elec. connected with the printed **circuit** conductor via **wire** bonding. A signal-transduction **circuit** conductor on the printed **circuit** board is connected with a **circuit** conductor at the opposite side of the board or a **solder ball** -connecting **circuit** pad via plated through-**holes** and is wholly sealed with a **resin**. The metal sheet with a little larger size than the printed **circuit** board placed at the center (to the thickness direction) is elec. insulated with a thermosetting **resin** compn. and has .gtoreq.1 elec. insulated clearance **holes** (larger than the through **hole**). A part or whole periphery of the metal sheet is exposed at the back of the **circuit** board and some metal notches with the same size as the fixing area of the semiconductor devices are projected for heat release. The package shows improved reliability.

L11 ANSWER 24 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 1999:498845 HCAPLUS

DN 131:178569

TI Peripheral heat-release semiconductor plastic package

IN Oka, Morio; Ikeguchi, Nobuyuki; Yamane, Kozo

PA Mitsubishi Gas Chemical Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 9 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

04/10/2002

Serial No.:09/852,847

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11220062	A2	19990810	JP 1998-34232	19980130
AB	<p>A semiconductor chip is fixed on an exposed metal sheet at the center on one side of a printed circuit board and the chip is elec. connected with the printed circuit conductor via wire bonding. A signal-transduction circuit conductor on the printed circuit board is connected with a circuit conductor at the opposite side of the board or a solder ball-connecting circuit pad via plated through-holes and is wholly sealed with a resin. The metal sheet with a little larger size than the printed circuit board placed at the center (to the thickness direction) is elec. insulated with a thermosetting resin compn. and has .gtoreq.1 elec. insulated clearance holes (larger than the through hole). A part or whole periphery of the metal sheet is exposed at the face and back of the circuit board and some metal notches with the same size as the fixing area of the semiconductor devices are projected for heat release. The package shows improved reliability.</p>				

L11 ANSWER 25 OF 33 HCAPLUS COPYRIGHT 2002 ACS
 AN 1999:498844 HCAPLUS
 DN 131:178568
 TI Cavity-type semiconductor plastic packages with good heat releasability and heat resistance after moisture absorption
 IN Take, Morio; Ikeguchi, Nobuyuki; Yamane, Kozo
 PA Mitsubishi Gas Chemical Co., Ltd., Japan
 SO Jpn. Kokai Tokkyo Koho, 9 pp.
 CODEN: JKXXAF
 DT Patent
 LA Japanese
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11220061	A2	19990810	JP 1998-34231	19980130
AB	<p>A semiconductor chip is fixed on an exposed concave metal sheet at the center on one side of a printed circuit board and the chip is elec. connected with the printed circuit conductor via wire bonding. A signal-transduction circuit conductor on the printed circuit board is connected with a circuit conductor at the opposite side of the board or a solder ball-connecting circuit pad via plated through-holes and is wholly sealed with a resin. The metal sheet with a little larger size than the printed circuit board placed at the center (to the thickness direction) is elec. insulated with a thermosetting resin compn. and has .gtoreq.1 elec. insulated clearance holes (larger than the through hole). A part of the metal is exposed at the center of the circuit board and some metal sheets are projected from the clearance holes for heat release. The package shows improved reliability.</p>				

L11 ANSWER 26 OF 33 HCAPLUS COPYRIGHT 2002 ACS
 AN 1999:77418 HCAPLUS
 DN 130:147302
 TI Printed **wiring** board having **bump electrode** and its production method.
 IN Nakamura, Yoshifumi; Itagaki, Minehiro; Takezawa, Hiroki; Bessho, Yoshihiro; Shiraishi, Tsukasa

04/10/2002

Serial No.:09/852,847

PA Matsushita Electric Industrial Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 10 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11026902	A2	19990129	JP 1997-173870	19970630
	US 2001029666	A1	20011018	US 2001-873461	20010605
PRAI	JP 1997-173870	A	19970630		
	US 1998-106302	A3	19980629		

AB A printed **wiring** board having a strongly bonded **bump electrode** comprises a via-hole conductor from a conductor paste in the via **hole** of an insulator **resin** board and a **bump electrode** from a hardened conductor paste on the via-hole conductor. A method for fabricating the board involves filling a via **hole** of a transfer sheet with a conductor paste, transferring the conductor paste on the via-hole conductor of an insulator **resin** board, and hardening the conductor paste. Specifically, the conductor paste may contain Ag, Au, Cu, Pd, Sn, Pb, Ni, or their alloys.

L11 ANSWER 27 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 1999:164636 HCAPLUS

DN 130:289724

TI Flip **chip** MPU module on high performance printed **circuit** board "ALIVH"

AU Shiraishi, Tsukasa; Amami, Kazuyoshi; Bessho, Yoshiriro; Sakamaoto, Kazunori; Eda, Kazuo; Ishida, Toru; Fukuoka, Kazuyoshi

CS Matsushita Electric Industrial Co., Ltd., Osaka, 571-8501, Japan

SO Proc. - Int. Conf. Multichip Modules High Density Packag. (1998), 520-525
Publisher: Institute of Electrical and Electronics Engineers, New York, N. Y.

CODEN: 67JBA3

DT Conference

LA English

AB This paper describes of a flip **chip** MPU (microprocessor unit) module on a high performance printed **circuit** board "ALIVH (Any Layer Inner Via **Hole** Structure)" for sub-note PCs using modified SBB (**Stud Bump** Bonding) technique. The SBB technique is an advanced flip-**chip** bonding technique, for high d. Multi-**Chip**-Modules (MCMs), which can mount bare LSI **chips** directly onto substrates. The structure of bonding portion is composed of Au bumps having two-stepped construction and conductive adhesives. The ALIVH substrate is a high d. and high performance multi-layered printed **wiring** board with any layer inner via **hole** structure, via **hole** processing technol. using a CO2 laser and interconnection technol. that employs conductive paste. In this fabricated MPU module, 4 LSI **chips** are mounted onto 8 layered ALIVH substrate and the clock frequency is 160MHz. The wt. of it was reduced 40% of the conventional one.

RE.CNT 6 THERE ARE 6 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L11 ANSWER 28 OF 33 INSPEC COPYRIGHT 2002 IEE

AN 1997:5704132 INSPEC DN B9711-0170J-022

TI Development of highly reliable CSP.

AU Yamaji, Y.; Juso, H.; Ohara, Y.; Matsune, Y.; Miyata, K.; Sota, Y.; Narai,

A.; Kimura, T.; Fujita, K.; Kada, M. (VLSI Dev. Lab., Sharp Corp., Nara, Japan)
SO 1997 Proceedings. 47th Electronic Components and Technology Conference (Cat. No.97CH36048)
New York, NY, USA: IEEE, 1997. p.1022-8 of 1294 pp. 4 refs.
Conference: San Jose, CA, USA, 18-21 May 1997
Sponsor(s): Components, Packaging, & Manuf. Technol. Soc. IEEE; Electron. Ind. Assoc
Price: CCCC 0 7803 3857 X/97/\$4.00
ISBN: 0-7803-3857-X
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB High density packages are demanded due to recent miniaturization for personal tools. In order to satisfy these demands, development is being done in various companies in CSP (**Chip-Size-Package** or **Chip-Scale-Package**) in which its package size is nearly the same as LSI **chip** and function is close to bare **chip**. We have developed and mass production of CSP using current equipment based on a proven packaging technology involving **wire** bonding and transfer mold technology. We can realize 0.8 mm terminal pitch and from the memory with a few to ASIC with 300 in pin counts using this technology and correspond to various matrix layout independent of LSI **chip** size. The CSP developed by us uses polyimide with one side pattern. After mounting the LSI **chip** and connecting with **wire** bonding, one side is contained with mold **resin**. External terminals use **solder ball** which is of area array structure. In order to minimize the outline size of the package to be as close to the LSI **chip** as possible, various technologies were developed such as ultra-short loop **wire** bonding technology of a half length compared to conventional loop length, super-small **solder ball** mounting technology how far size of 0.3 mm ϕ , low stress high precision cutting technology with laser and fine pattern technology of substrate. Furthermore, in order to maintain high reliability to the level attained in conventional plastic packages, development was done on thermally resistant insulator and on mold **resin** which increase the adherence with substrate. Work was also done to reduce the effect of moisture in package through vent **hole** in pattern substrate. Regarding mounting to the PCB, the CSP developed by us is able to be mounted by merely recognizing of package's high precision outline with laser cutting technology and mounting with other packages is possible due to collective reflow which utilize conventional technologies. Reliability evaluation after mounting has shown that it is very realistic levels for us. By developing the above technologies and developing new materials, packaging technology for a highly reliable CSP was made possible.

L11 ANSWER 29 OF 33 HCAPLUS COPYRIGHT 2002 ACS
AN 1997:708874 HCAPLUS
DN 128:29125
TI MCM-ALIVH using SBB flip-**chip** bonding technique
AU Amami, Kazuyoshi; Yuhaku, Satoru; Shiraishi, Tukasa; Bessho, Yoshihiro; Sakamoto, Kazunori; Eda, Kazuo; Ishida, Toru
CS Matsushita Electric Industrial Co., Ltd., Osaka, 571-8501, Japan
SO Proc. SPIE-Int. Soc. Opt. Eng. (1997), 3235(Proceedings 1997 International Symposium on Microelectronics, 1997), 278-283
CODEN: PSISDG; ISSN: 0277-786X
PB SPIE-The International Society for Optical Engineering

DT Journal
 LA English
 AB The authors have developed a multi-**chip** module (MCM) using **stud-bump** bonding (SBBTM) flip-**chip** bonding technique onto an ALIVHTM (any layer inner via **hole** structure) substrate. The SBB technique is an advanced flip-**chip** bonding technique, for high d. Multi-**Chip**-Modules (MCMs), which can mount bare LSI **chips** directly onto substrates. The structure of the bonding portion is composed of Au bumps having two-stepped construction and conductive adhesives. The conductive adhesive is very flexible in bond, thus relating thermal and mech. stresses. The ALIVH substrate was developed in the authors' lab. It is a high d. and high performance multi-layered printed **wiring** board with any layer inner via **hole** structure, via **hole** processing technol. using a CO2 laser and interconnection technol. that employs conductive paste. The authors had good results for several reliability tests in the test vehicles of MCM-ALIVH. Esp., in the thermal shock test, the increase of connecting resistance in MCM-ALIVH was smaller than that of MCM-Ls which used ordinary org. substrates in stead of the ALIVH substrate. The authors had manufd. CCD camera module using MCM-ALIVH. Three LSI **chips** had been mounted on the sir-layered ALVH substrate. The obtained MCM-ALIVH realized down-sizing (60% down) and light-weighting (30% light) comparing with the conventional module. And the elec. characteristics of newly manufd. CCD camera module were equal to the conventional module.

L11 ANSWER 30 OF 33 INSPEC COPYRIGHT 2002 IEE
 AN 1996:5455504 INSPEC DN B9702-2860C-003
 TI New packaging technology for SAW device.
 AU Ando, D.; Oishi, K.; Nakamura, T.; Umeda, S.; Yuzawa, T. (Corp. Components Dev. Centre, Matsushita Electron. Components Co. Ltd., Osaka, Japan)
 SO 1995 Japan IEMT Symposium. Proceedings of 1995 Japan International Electronic Manufacturing Technology Symposium (Cat. No.95CH35994) New York, NY, USA: IEEE, 1996. p.403-6 of xvi+480 pp. 7 refs. Conference: Omiya, Japan, 4-6 Dec 1995
 Sponsor(s): Steering Committee of 1995 Japn IEMT Symposium; IEEE Tokyo Sect.; Tokyo Chapter of IEEE CPMT Soc.; Found. Adv. Int. Sci.; IEICE; IEE of Japan; Microelectron. Soc.-Japan; Japan Inst. Interconnecting & Packaging Electron. Circuits; Soc. Instrum. & Control Eng.; Japan Soc. Precision Eng.; Japan Welding Soc.; Japan Technol. Transfer Assoc.; Japan Electron. Mater. Soc.; Japan Soc. Applied Phys.; Soc. Polymer Sci., Japan; Japan Inst. Metals; Ceramic Soc. Japan; Optoelectron. Ind. & Technol. Dev. Assoc.; Electrochem. Soc. Japan; IEEE Electron. Device Soc. Tokyo Chapter; SEMI, Japan; LEOS-Laser Opt. Soc. Tokyo Chapter
 ISBN: 0-7803-3622-4

DT Conference Article
 TC New Development; Experimental
 CY United States
 LA English
 AB A new hermetic seal package using glass **wafers** for surface acoustic wave (SAW) device was developed. Two glass **wafers** are used. Cavity and through **hole** are formed on each glass **wafer** by the grinding process. Two glass **wafers** are combined in atomic level by using the glass direct bonding technique. The SAW device **chip** is inserted into the cavity. Electrodes are taken out from through **holes** by **solder balls** without using **wires**. These technologies were applied to SAW resonator. The size of developed SAW resonator is 4.0*2.0*0.8 mm. The characteristics and reliability of developed SAW resonator were

investigated. The characteristics degradation by packaging process was not observed. Insertion loss was improved due to wireless assembly, and the characteristics change after high temperature preservation test was extremely small because there is no **resin** in the glass package.

- L11 ANSWER 31 OF 33 INSPEC COPYRIGHT 2002 IEE
AN 1994:4776050 INSPEC DN B9411-0170J-024
TI Capturing design advantages of BGAs.
SO Surface Mount Technology (March 1994) vol.8, no.3, p.36-7, 43. 0 refs.
Price: CCCC 0893-3588/94/\$1.00+50
ISSN: 0893-3588
DT Journal
TC Application; Practical
CY United States
LA English
AB The construction of the over-molded pad array carrier (OMPAC) begins with a single-layer BT **resin** epoxy PCB. The **die** is attached via a gold-plated **die** attach and a silver-filled epoxy. Conventional plastic transfer molding encapsulated the package and interconnection between **die** and epoxy PCB is through thermosonic gold **wire** bonding. From there copper traces are routed to an array of metal pads on the bottom side of the board to which solder bumps (62 Sn, 36 Pb, 2 Ag) are partially reflowed, providing the package with 'leads.' For increased heat dissipation, OMPACs include thermal vias (copper plated-through **holes**) directly beneath the **die**. Copper foil serves to distribute the heat to specific **solder balls**, which are connected to the system PCB (product) ground plane(s).
- L11 ANSWER 32 OF 33 INSPEC COPYRIGHT 2002 IEE
AN 1994:4805087 INSPEC DN B9412-2210D-012
TI Soldering evaluations of organic solderability preservatives.
AU Wenger, G.M.; Machusak, D.A. (AT&T Bell Labs., Princeton, NJ, USA)
SO Proceedings of the Technical Program. NEPCON West'93
Des Plaines, IL, USA: Reed Exhibition Companies, 1993. p.436-451 vol.1 of 3 vol. 2022 pp. 10 refs.
Conference: Anaheim, CA, USA, 7-11 Feb 1993
DT Conference Article
TC Practical; Experimental
CY United States
LA English
AB Organic solderability preservative (OSP) coatings are used as alternatives to hot air solder leveled (HASL) tin/lead (Sn/Pb) to provide solderable copper surfaces for printed **wiring** board (PWB) assembly wave soldering. Until recently, OSP coatings were either thick (3-5 microns) rosin or **resin** based pre-flux or relatively thin (30-300 angstroms) organic nitrogen azole compounds which protect copper by chemically bonding to it, thus preventing a copper-oxygen reaction. The pre-flux coatings are difficult to electrically test through and need to be removed in a **post** wave **solder** cleaning operation. Azole compounds, such as benzotriazole and imidazole, have been successfully used in the past for copper corrosion protection and for wave soldering of through-**hole** components using water soluble flux (WSF). Cleaning is therefore a necessary part of the assembly process with either type of OSP coating. In this paper, the results of solderability testing and soldering evaluations using test vehicles coated with various OSP coatings are reported. The coatings are separated into three types of materials and referred to by letter designation; azoles applied as monolayer films (AZ), azoles applied to thicker (1000-5000 angstrom) films

04/10/2002

Serial No.:09/852,847

(MA), and pre-fluxes (PF).

L11 ANSWER 33 OF 33 HCAPLUS COPYRIGHT 2002 ACS

AN 1969:434455 HCAPLUS

DN 71:34455

TI Controlled-collapse reflow **chip** joining

AU Miller, Lewis F.

CS IBM Components Div. Lab., East Fishkill, N. Y., USA

SO IBM J. Res. Develop. (1969), 13(3), 239-50

CODEN: IBMJAE

DT Journal

LA English

AB Connecting joints were formed by the controlled-collapse wet solder reflow process. Ductile pads were formed by application of 25 Pb-5 Sn to the elec. contact pads of Si devices by vacuum metallizing in an oversized area around the pad and then heating to form a hemispherical ball (4-5 mils in diam.) by reflow at 340.degree.. The devices and modules, which were self-aligning, were joined in reflow furnaces contg. inert or reducing atm. Any irregularly shaped pads were reformed into hemispheres by the reflow process. The solder was restricted by the dot and dam processes. The **circuit** pattern was screened on the substrate with non-tinnable electrode paste, dried, and fired, followed by deposition of tinnable electrode paste and passive components. The devices with **solder pads** were then reflow bonded to the isolated tinned spots. Surface tension support prevented collapse and shorting at the device **edges**. The method can be inversed by depositing the untinned lands first. In the dam method, the ends of the normal screen and fired tinnable land were delineated with nontinnable barriers. Extra pads may be added. Tinnable lands may consist of 80 Ag:20 Pd, Au:Pt, Ag:Au:Pd, and Au:Pt:Pd; the same material can be used for non-tinnable lands by adding 1-4% untinning agents such as colloidal silica, organometallics, polymers, frit, or metals. The diln. effect was not crit. Preferably, dams were formed of nonconductive material such as glass, polyimide **resins**, and colloidal silicas. The **chip** joining yield was >97% and the joint tensile strength was 50 g./pad. Devices of the order of 60-80 mils sq. having module **lines** and spaces of 4 mils can be manufd. The method can be extended to thin-film technology and normal Cu-clad printed **circuits**.

L17 ANSWER 1 OF 21 INSPEC COPYRIGHT 2002 IEE
 AN 1998:5932661 INSPEC DN B9807-2250-010; C9807-5430-007
 TI MCM-L/D for mobile computer.
 AU Hirano, Y.; Fujii, A.; Tsunoi, K.; Baba, S. (Fujitsu Labs. Ltd., Kawasaki, Japan)
 SO Proceedings. 1997 International Symposium on Microelectronics (SPIE vol.3235)
 Reston, VA, USA: IMAPS - Int. Microelectron. & Packaging Soc, 1997.
 p.250-5 of xvii+707 pp. 3 refs.
 Conference: Philadelphia, PA, USA, 14-16 Oct 1997
 Sponsor(s): IMAPS - Int. Microelectron. & Packaging Soc
 ISBN: 0-930815-50-5
 DT Conference Article
 TC Practical; Experimental
 CY United States
 LA English
 AB We have developed MCM-L/D for mobile PCs. The MCM-L/D consists of a CPU, a PCI set, a cache, and a power supply section. It incorporates four **dies**, one of which has a minimum **connection** pitch of 85 mu m. The **dies** are **connected** to a printed-circuit substrate using flip-**chip** bonding technology. The size of the MCM is 50*50 mm. A **wire** bonding method is used to form Au bumps on the **dice**. Each **die** is pushed against a printed-circuit substrate so that the bumps are **electrically connected** to electrodes on the substrate. An insulating adhesive is then used to affix and seal the **die**. Conductive paste is applied between the Au **bumps** and the substrate **electrodes** to enhance **connectivity** and increase reliability. The technology we developed secures the reliable **connections** using adhesive. As the reliability of this adhesive is so important, we investigated its properties. We also investigated the deformation properties of the MCM-L/D substrate to optimize the flip **chip mounting** pressure. The **connection** pitch is getting smaller (from 120 mu m early on to 85 mu m recently) year by year. This trend is likely to continue. We are also developing a technology to meet the demand for smaller pitches (such as 60 mu m). We have succeeded in reducing both the size and weight of the MCM-L/D to one-fourth. We also conducted a feasibility study on smaller pitches (such as 60 mu m).

L17 ANSWER 2 OF 21 HCAPLUS COPYRIGHT 2002 ACS
 AN 2002:155703 HCAPLUS
 DN 136:176744
 TI Manufacture method of semiconductor package with removal of flash resin residues
 IN Kwak, Jae Seong; Ryu, Sang Hyeon; Lee, Jae Hak
 PA Amkor Technology Korea, Inc., S. Korea
 SO Repub. Korean Kongkae Taeho Kongbo, No pp. given
 CODEN: KRXXA7
 DT Patent
 LA Korean
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 2000038064	A	20000705	KR 1998-52924	19981203
AB	A manufg. method of a semiconductor package is provided to effectively remove a flash resin residue on leads. In a semiconductor package, a semiconductor chip is mech. attached onto a chip -				

mounting pad by an adhesive such as epoxy and elec. connected with half-etched leads beside the chip-mounting pad by wires. An encapsulant covers the chip, the leads, the wires, and the chip-mounting pad, except lower portions of the leads and chip-mounting pad, on which solder balls will be formed. However, the lower portions of the leads and chip-mounting pad are coated with an undesirable flash, i.e., a resin residuum of the encapsulant. A laser beam used in a marking process is therefore used to remove the flash. The lower portions of the leads and chip-mounting pad are partially cut by the laser beam, so that the flash is effectively removed without using any addnl. equipment.

L17 ANSWER 3 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:798729 HCAPLUS

DN 135:326247

TI High-density electronic packages fabricated at low cost with easy mounting

IN Urushima, Michitaka

PA Japan

SO U.S. Pat. Appl. Publ., 28 pp.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001036711	A1	20011101	US 2001-839298	20010423
PRAI	JP 2000-123306	A	20000424		

AB Semiconductor device comprises semiconductor chip, Au ball bumps formed on pad electrodes with a stud bump method, and thermoplastic adhesive layer provided on the surface of semiconductor chip on which pad electrodes are formed, in which the tops of Au ball bumps projecting from the surface of adhesive layer. Reliable bonding can be realized by forming the bumps for elec. connection and the adhesive resin having an adhesion function on the semiconductor chip. In addn., the present invention provides a method of bonding a Cu foil to a semiconductor wafer to form a wiring pattern, a multi chip module in which elec. connection is established by bumps bonded to each other through an adhesive layer, and the like.

L17 ANSWER 4 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:762681 HCAPLUS

TI Semiconductor device and its production method. [Machine Translation].

IN Fujimoto, Hiroaki; Nomura, Toru

PA Matsushita Electric Industrial Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 12 pp.
CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001291818	A2	20011019	JP 2000-106034	20000407

AB [Machine Translation of Descriptors]. In case of 1 tip/chip structure, correspondence to the semiconductor equipment component which

future diversifies and decrease of number of articles with the loading device not be able to correspond to the multi-function semiconductor device to the miniaturization and light weight conversion of the electronic equipment with that cannot correspond. 1st semiconductor component through 8 and **bump electrode** 9, the 2nd semiconductor component 10 which is **connected** and, 3rd semiconductor component through 11 and **bump electrode** 12, as possesses with the 4th semiconductor component 13 which, is **connected** the base of 1st semiconductor component 8 and the base of 3rd semiconductor component 11 adhesion by adhesion component 14, the formation it does laminate structure, is **mounted** on insulated baseplate 15, is **connected electrically** in metal thin line 17, appearance of insulated baseplate 15 is sealed with insulated seal resin 18 of the epoxy system with the semiconductor device where Certain. With this structure, the many functions due to multichip structures can be actualized, the semiconductor device of high density **mounted** type can be actualized.

L17 ANSWER 5 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:664608 HCAPLUS

TI Semiconductor package having enhanced ball grid array protective dummy members

IN Sato, Akira

PA Nec Corporation, Japan

SO U.S., 14 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6287895	B1	20010911	US 2000-493198	20000128
PRAI	JP 1999-21030	A	19990129		

AB A semiconductor package having: a **chip-sized wiring** board that has a predetermined **wiring** pattern; a semiconductor **chip** that is **mounted** on the **wiring** board and is **electrically connected** to the **wiring** pattern; sealing resin that seals at least the **connection** part of the **wiring** board and the semiconductor **chip**; an array of **solder balls** for external **circuit connection** that are **connected** through an opening in the sealing resin to a land of the **wiring** pattern; and a protective member that is disposed along at least two sides of the surface where the array of **solder balls** are provided.

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

=> D BIB AB 6-21

L17 ANSWER 6 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:636430 HCAPLUS

TI **Mounting** structure of semiconductor device and **mounting** method thereof

IN Miyazaki, Hirokazu

PA Nec Corporation, Japan

SO U.S. Pat. Appl. Publ.

CODEN: USXXCO

DT Patent

04/10/2002

Serial No.:09/852,847

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2001017425	A1	20010830	US 2001-788596	20010221
	JP 2001244297	A2	20010907	JP 2000-49904	20000225
PRAI	JP 2000-49904	A	20000225		

AB An insulating sheet which **connects** a semiconductor **chip** and a **wiring** substrate is provided between the semiconductor **chip** and the **wiring** substrate. The insulating sheet has windows therethrough at positions corresponding to those of **connection** pads of the **wiring** substrate and has leads, one end of each of the leads being fixed on the sheet and the other end of each of the leads protruding from the opposite surface of the sheet through a window. Each of **solder balls** of the semiconductor **chip** is **connected** to the fixed one end of one of the leads, and each of the **connection** pads is **connected** to the other end of each of the leads to **electrically connect** the semiconductor **chip** and the **wiring** substrate.

L17 ANSWER 7 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:564300 HCAPLUS

DN 135:130730

TI Electric **circuit** boards for packaging semiconductor devices

IN Matsudera, Hiroshi

PA Kyocera Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001210928	A2	20010803	JP 2000-23346	20000127

AB The title **circuit** boards comprise (1) a semiconductor package-**mounted** insulative substrate, (2) **circuit wires** **connected** from the packages to **connecting** round pads provided on the rear surface of the substrate, and (3) an external **circuit** board having pads to be **connected** with a low-m.p. Pb-free **solder** to the **pads** provided on rear surface of the substrate. The round pads have grooves near their periphery and plated on their surface successively with a Ni layer, a Pd-P layer, and a Au (thickness 0.03-0.5 .mu.m) layer. The grooves on the pads and the plated layers prevent thermal stress-caused cracks on the **connecting** pads.

L17 ANSWER 8 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:421698 HCAPLUS

TI Semiconductor device comprised of a ball grid array and an insulating film with preformed land openings

IN Ichinose, Michihiko

PA Nec Corporation, Japan

SO U.S., 10 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
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04/10/2002

Serial No.:09/852,847

PI	US 6246117	B1	20010612	US 1999-460696	19991214
PRAI	JP 1998-356169	A	19981215		

AB A semiconductor device of a BGA (Ball-Grid-Array) package comprises a lead frame, a semiconductor **chip**, bonding **wires**, a plastic, an insulation film, and **solder balls**. The semiconductor **chip** is **mounted** on one side of the lead frame, and is **electrically connected** to the lead frame by the bonding **wires**. The plastic encapsulates the semiconductor **chip** and the bonding **wires**. The insulation film has openings for exposing predetermined regions of the lead frame. The insulation film is affixed onto an underside surface of the lead frame. The **solder balls** act as **connection terminals**. The **solder balls** are formed on the regions of the lead frame exposed through the openings in the insulation film.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 9 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:312469 HCAPLUS
DN 134:319738
TI Plastic ball grid array package with strip **line** configuration
IN Juneja, Nitin; Thuraiarajaratnam, Aritharan
PA Lsi Logic Corporation, USA
SO U.S., 7 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	-----	----	-----	-----	-----
PI	US 6225690	B1	20010501	US 1999-467081	19991210

AB A semiconductor package is disclosed. According to one embodiment, the package comprises a substrate having a top surface with traces thereon and a bottom surface with **solder balls** thereon, the substrate comprising .gtoreq.3 material layers defining .gtoreq.4 substantially planar metal layers, in which one of the metal layers comprises a ref. layer that serves as a ref. to both traces on a metal layer above the ref. layer and traces on a metal layer below the ref. layer. A semiconductor **die** is **mounted** to the substrate and bonding **wires elec. connect** the semiconductor **die** to the traces on the top surface of the substrate. The traces on the top surface of the substrate are **elec. connect** to the **solder balls** through vias and possibly through routing on another metal layer.

RE.CNT 14 THERE ARE 14 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 10 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:295002 HCAPLUS
DN 134:304203
TI Design and fabrication of a **stack** package for a semiconductor memory device
IN Park, Sang Wook; Cho, Soon Jin
PA Hyundai Electronics Industries Co., Ltd., S. Korea
SO U.S., 14 pp.
CODEN: USXXAM
DT Patent

04/10/2002

Serial No.:09/852,847

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6222259	B1	20010424	US 1999-393869	19990910
	KR 2000019697	A	20000415	KR 1998-37931	19980915
PRAI	KR 1998-37931	A	19980915		

AB Disclosed are a **stack** package and a method of manufg. the same. The **stack** package of the present invention comprises a ceramic capsule. A pair of protruding portions are formed at both upper sides of the ceramic capsule. A 1st semiconductor **chip** is attached on the upper face of the ceramic capsule and a 2nd semiconductor **chip** is attached on a lower face of the ceramic capsule. The 1st and 2nd semiconductor **chips** are disposed such that their bonding pads are disposed upwardly, more particularly the 2nd semiconductor **chip** has a size that its bonding pad may be exposed from both sides of the ceramic capsule. It is preferable to attach a heat sink at the lower face of the 2nd semiconductor **chip**. The 1st and 2nd semiconductor **chips** are **elec. connected** with a metal **wire**. A midway portion of the metal **wire** is laid on the protruding portion of the ceramic capsule. The entire resultant is encapsulated with a molding compd. while exposing the portion of metal **wire** laid on the protruding portion and the heat sink. A conductive bump is formed on the exposed portion of the metal **wire**, and a **solder ball** is **mounted** on the conductive bump.

RE.CNT 21 THERE ARE 21 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 11 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:220435 HCAPLUS

TI Process for **mounting** electronic device and semiconductor device

IN Imasu, Satoshi; Yoshida, Ikuo; Hayashida, Tetsuya; Yamagiwa, Akira; Takeura, Shinobu

PA Hitachi, Ltd., Japan; Hitachi Hokkai Semiconductor, Ltd.

SO U.S., 24 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6208525	B1	20010327	US 1998-48054	19980326
PRAI	JP 1997-75970	A	19970327		

AB An electronic device comprising a semiconductor **chip** which is fixed to the **mounting** face of a **wiring** board through an adhesive and in which external terminals are **electrically connected** with electrode pads of the **wiring** board through **bump electrodes**. Recesses are formed in the electrode pads, and in the recesses the **electrode** pads and the **bump electrodes** are **connected**. The electrode pads are formed over the surface of a soft layer, and the recesses are formed by elastic deformation of the electrode pads and the soft layer.

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 12 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:865974 HCAPLUS

TI Semiconductor device having an insulating substrate

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Serial No.:09/852,847

IN Takashima, Akira; Taniguchi, Fumihiko; Higashiyama, Toshihisa
PA Fujitsu Ltd., Japan
SO U.S., 13 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6160313	A	20001212	US 1999-274939	19990323
PRAI	JP 1998-87003	A	19980331		

AB A semiconductor device includes an insulating substrate; a semiconductor **chip mounted** on a front surface of the insulating substrate and provided with electrode pads; bonding pads provided on the front surface of the insulating substrate and **electrically connected** to the semiconductor **chip** by means of **wires**; ball bumps provided on a back surface of the insulating substrate in rows in a grid-like manner; electrode patterns provided in rows on the front surface of the insulating substrate so as to correspond to positions of the **ball bumps**, respectively, the **electrode** patterns being **connected** to the ball bumps through holes formed in the insulating substrate; and interconnection patterns **electrically connecting** the bonding pads and the electrode patterns. The bonding pads may be provided in a plurality of rows, each of the rows being provided between one of neighboring pairs of rows of the electrode patterns. Alternatively, the bonding pads may be provided in a staggered manner between one of neighboring pairs of rows of the electrode patterns.

RE.CNT 5 THERE ARE 5 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 13 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 2000:781288 HCAPLUS
TI **Circuit** board with terminals having a solder lead portion
IN Sato, Shingo; Matsuzono, Seigo; Nakamura, Kenshi
PA Kyocera Corporation, Japan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6143992	A	20001107	US 1998-160105	19980924
PRAI	JP 1997-262404	A	19970926		

AB A **circuit** board of the invention comprises an insulating base, which has a semiconductor element **mounting** portion on an top or bottom side thereof, and on which **wiring** patterns led out of the semiconductor element **mounting** portion are installed; and a plurality of substantially circular terminal pads, which are formed on the bottom side of the insulating base, which are **connected** to the **wiring** patterns, and to which solder terminals will be **joined**, wherein each of the terminal pads is provided with a solder lead portion which projects from a center side toward a perimeter side of the insulating base in a diametrical direction of the terminal pad. A part of the solder terminal is pulled out at the solder lead portion, whereby it is possible to prevent a fatigue failure of a **joint** of the terminal **pad** and the **solder** terminal due to a concentration of thermal stress, to **electrically**

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connect the solder terminal to the terminal pad in a stable manner for a long time period.

RE.CNT 3 THERE ARE 3 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L17 ANSWER 14 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:638699 HCAPLUS

TI Driver IC **mounted** module. [Machine Translation].

IN Kawata, [NAME NOT TRANSLATED]; Aoki, [NAME NOT TRANSLATED]; Koizumi, Haruo

PA Fujitsu Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 29 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000250425	A2	20000914	JP 1999-49121	19990225
AB	[Machine Translation of Descriptors]. Holding down the impedance of the line of drive voltage type wiring inside module low in regard to the driver IC mounted module which forms the drive circuit of the display which uses the flat plate display panel, it designates that assures the stabilization of indication operation as purpose. Control type wiring which supplies various signals in order driver IC tip/ chip 9 in order to drive the indicatory electrode of the flat plate display panel and driver IC tip/ chip 9 possesses with the wiring baseplate in order to connect electrically , at least, is inputted by driver IC tip/ chip 9 and is inputted to the 1st wiring section 1 where drive electrical power system wiring which supplies the power source voltage in order to drive the flat plate display panel by way of the driver IC tip/ chip was formed and and driver IC tip/ chip 9 to control driver IC tip/ chip 9 the formation the 2nd wiring section 2 which is done and the driver IC tip/ chip Is guided from 9 and as output terminal wiring in order to connect to the indicatory electrode of the flat plate display panel had with the 3rd wiring section 3 which the formation is done, constitutes.				

L17 ANSWER 15 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:502265 HCAPLUS

DN 133:98017

TI Semiconductor device and the manufacture method

IN Choe, Jong-kon

PA Samsung Electronics Co.,ltd., S. Korea

SO Repub. Korea, No pp. given

CODEN: KRXXFC

DT Patent

LA Korean

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	KR 9702135	B1	19970224	KR 1993-27319	19931211
AB	A semiconductor device is provided which is constructed in such a manner that a plurality of wire patterns for elec. connection of various signal lines are formed on a				

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plastic substrate in which slots for **stacking** a plurality of substrates vertically are formed, a **die pad** for **mounting** a semiconductor **chip** is formed, being surrounded by the **wire patterns**, through holes are formed in zigzag to allow the upper and lower layers of the substrate to be **elec. connected** to winding portion of the **wire patterns**, and **solder balls** are formed on the backside of the substrate after molding. .gtoreq.1 **Solder ball** is formed in the contact holes of the lower layer of the plastic substrate after a metal line for short-circuiting the **wire patterns** is formed. Accordingly, high-d. packaging is realized.

L17 ANSWER 16 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:618577 HCAPLUS
TI **Solder ball grid array carrier package with heat sink**
IN Oh, Sang Eon
PA Samsung Electronics Co., Ltd., S. Korea
SO U.S., 6 pp., Cont. of Ser. No. US 1996-755098, filed on 25 Nov 1996, now abandoned
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5959356	A	19990928	US 1997-953381	19971017
PRAI	KR 1995-43760		19951125		
	US 1996-755098		19961125		

AB A **solder ball** grid array carrier package has a **circuit board** with conductive wirings and a plurality of through holes. At least one semiconductor **chip** is **mounted** on an upper surface of the **circuit board** and bonding **wires electrically connect** the **chip** to the conductive wirings. A plurality of **solder balls** are **electrically connected** to the conductive wirings, with the **solder balls** being adhered to a lower surface of the **circuit board**. A heat sink is also adhered to the lower surface of the **circuit board**. The heat sink is in direct contact with the through holes of the **circuit board**, with the through holes allowing for heat dissipation.

L17 ANSWER 17 OF 21 HCAPLUS COPYRIGHT 2002 ACS
AN 1999:610937 HCAPLUS
DN 131:236737
TI Structure and method for packaging of semiconductor device.
IN Kusamitsu, Hideki
PA NEC Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 6 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 11260945	A2	19990924	JP 1998-59433	19980311
	JP 3132458	B2	20010205		

AB A semiconductor device packaging structure is described, which comprises a bare-chip **circuit element mounted** on a **wiring board** to **elec. connect** desired portions

of the element and board with **bump electrodes**. A reinforcement material (such as Al or AlN) wider than the bare-**chip circuit** element is provided at the back of the element via a resin layer to form a hollow structure. Specifically, the resin layer may comprise a UV-curing resin layer and the bare-**chip circuit** element may comprise GaAs. A packaging method using the above structure is also described.

L17 ANSWER 18 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 1998:508896 HCAPLUS

DN 129:143808

TI Production of a semiconductor device package having a semiconductor **chip mounted** face down on a substrate with protruding electrodes

IN Ohida, Mitsuru; Aoki, Hideo; Iwasaki, Hiroshi

PA Kabushiki Kaisha Toshiba, Japan

SO U.S., 10 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5786271	A	19980728	US 1996-675213	19960703
PRAI	JP 1995-169644		19950705		

AB A semiconductor package has a **wiring circuit** contg. a conductive terminal formed on a 1st face of a ceramic substrate and a flat external **connecting** terminal **elec. connected** to the **wiring circuit** formed on a 2nd face. An electrode pad is formed on a 1st face of a semiconductor **chip**. This semiconductor **chip** is **mounted** on the substrate with its 1st face down to oppose the 1st face of the substrate. A ball **bump** as a protruding **electrode** formed on the conductive terminal of the substrate and a ball **bump** as a protruding **electrode** formed on the electrode pad of the semiconductor **chip** are **connected** by solid-phase diffusion. A sealing resin layer is formed in the space between the substrate and the semiconductor **chip**, with a 2nd face of the semiconductor **chip** exposed.

L17 ANSWER 19 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 1997:124251 HCAPLUS

DN 126:138615

TI **Mounting** semiconductor devices by gold bump contacts

IN Nobori, Kazuhiro; Nishida, Kazuto

PA Matsushita Electric Ind Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 8 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 08298271	A2	19961112	JP 1995-102759	19950426

AB The title process involves **elec.-mech. connecting** a capillary-mounted Au **wire-connected** Au ball on an **electrode** on the devices by hot-pressing by ultrasound vibration to give a Au projected contact on the electrode, leveling the top portion of the projected contact by pressing with a

leveling plate to give a stepped bump contact, laminating on a **circuit** substrate with an anisotropic elec. conductive film dispersed with conductive microparticles in an insulative polymer adhesive, and subsequently hot-pressing the device on the substrate by the bump contact, and hardening the anisotropic conductive polymer film. The process gives the **mounting** a secured **elec.** and mech. **connection**.

L17 ANSWER 20 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 1995:928510 HCAPLUS

DN 124:42425

TI **Chip** scale package: "a lightly dressed LSI **chip**"

AU Yasunaga, Masatoshi; Baba, Shinji; Matsuo, Mitsuyasu; Matsushima, Hironori; Nakao, Shin; Tachikawa, Toru

CS IC Assembly Engineering Department, Mitsubishi Electric Corporation, Itami, 664, Japan

SO IEEE Trans. Compon., Packag., Manuf. Technol., Part A (1995), Volume Date 1995, 18(3), 451-7

CODEN: IMTAEZ; ISSN: 1070-9886

DT Journal

LA English

AB A new flip-**chip**-like package named **chip** scale package (CSP) has been developed. It is constructed of LSI **chips**, thin resin coats, and **electrode balls**, having no leadframe nor any bonding **wires**. **Wiring** conductor patterns were used for **elec. connection** between internal pads on the **die** and external **electrode balls**. Also the transfer-bumping technique was applied for inner bump formation. Finally, solder **joint** life when **mounted** onto typical boards was estd. by simulation.

L17 ANSWER 21 OF 21 HCAPLUS COPYRIGHT 2002 ACS

AN 1993:460979 HCAPLUS

DN 119:60979

TI Electrically - conductive pastes and installing semiconductor devices on **circuit** boards

IN Nakatani, Seiichi; Betsusho, Yoshihiro

PA Matsushita Electric Industrial Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 04335545	A2	19921124	JP 1991-105472	19910510

AB An elec.-conductive paste for installing semiconductor device on **circuit** board is a mixt. of a Si, Ge, In, or Sn, powder (av. particle size of .ltoreq.10 .mu.m) and a soln. from an org. solvent and an org. Au salt. Installing a semiconductor device on a **circuit** board includes the steps of: (a) forming, with thermal energy, a ball at the tip of a metal **wire** (e.g., Au); (b) attacking the ball, with the use of a capillary, on the electrode pad of the semiconductor device; and moving the capillary in a loop and cutting the **wire** to create a doubly-protruded electrode; (c) pressing planar material to the tip of the protrusion to planarize it; (d) placing the elec.-conductive paste on a different substrate, and transferring the paste only onto the protrusion tips; (e) **mounting** the semiconductor device on the predetd. location of a **circuit** board with an elec.-conductive

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pattern; and (f) heating the **circuit** board to melt the
elec.-conductive paste and to **elec.-connect** the
protrusion tips with the elec.-conductive pattern.

L19 ANSWER 1 OF 6 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:72676 HCAPLUS

DN 136:127686

TI Semiconductor package and method of fabricating the same

IN Park, Kye Chan

PA S. Korea

SO U.S. Pat. Appl. Publ., 11 pp.

CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2002008315	A1	20020124	US 2001-858408	20010516
PRAI	KR 2000-42377	A	20000724		

AB A semiconductor package including a semiconductor **chip** having bonding pads resp. arranged in a **line** adjacent to 4 sides of the upper surface; Au bumps formed on each bonding pad; a glass substrate which is made by forming metal patterns, the metal pattern including an inner pattern **elec. connected** to the bonding pad of the semiconductor **chip** through the Au bumps, an outer pattern, and a connecting pattern between the inner pattern and the outer pattern: a Dam having a frame-shape on the connecting pattern and surrounding the inner patterns; sealing material sealing the space between the glass substrate around the semiconductor **chip** and **solder balls** attached on the outer patterns of each metal pattern.

L19 ANSWER 2 OF 6 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:380945 HCAPLUS

DN 134:360411

TI A high density hybrid **integrated circuit** package

having a flip-con structure with 90 percent decrease in packaging density and method of fabrication

IN Satyanarayana, Pappo; Yadagiri, Gunda; Goswami Krishna, Kumar

PA Indian Space Research Organisation, India

SO PCT Int. Appl., 19 pp.

CODEN: PIXXD2

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	WO 2001037332	A1	20010525	WO 2000-IN68	20000721
	W:				
	AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
	RW:				
	GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW, AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG				

PRAI IN 1999-MA1120 A 19991116

AB A high d. hybrid **integrated circuit** package comprising an insulator substrate (1) with a metalized pattern for interconnecting the **integrated circuit** configuration, an **integrated circuit flip chip** (7) consisting of

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plurality of semiconductor devices and provided with Au stud bumps (6) for providing interconnections by thermal compression bonding. The Au stud bumps (6) on the flip chip are bonded to the metalized portions on the ceramic substrate (1). An integrated circuit top chip (9) consisting of plurality of semiconductor devices is fixed with an epoxy (8) to the top portion of the flip chip (7) and the elec. connections from the top chip (9) to the metalized pattern (5) on the substrate (1) is taken through gold wires (4) bonded to the top chip (9) and the metalized pattern (5) on the substrate (1).

RE.CNT 7 THERE ARE 7 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L19 ANSWER 3 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:299938 HCAPLUS
TI Semiconductor device. [Machine Translation].
IN Osono, Takeaki
PA Mitsui High-Tec, Inc., Japan
SO Jpn. Kokai Tokkyo Koho, 7 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001118978	A2	20010427	JP 1999-298317	19991020
AB	[Machine Translation of Descriptors]. As for theme of this invention, the laminate the semiconductor chip of the optional quantity is possible without accompanying the enlargement of plane surface size to do, and also, there are times when the possible semiconductor device of the thing which achieves also shortening the lead time is offered. As the semiconductor device 1 which relates to this invention the baseplate one side of 10 where on one hand wiring pattern 11 was formed to the surface and said baseplate 10 the loading being done on the surface, wiring pattern 11 has with the semiconductor chip 2 which, is connected electrically at least semiconductor chip the resin seals the terminal area of 2 and wiring pattern and 11 becomes, makes the lead/read section 11 A which projecting from baseplate, 10 and package (resin seal section) 3 expands the portion of wiring pattern 11, provides solder ball 4 in the point of said lead/read section 11 A.				

L19 ANSWER 4 OF 6 HCAPLUS COPYRIGHT 2002 ACS
AN 2001:134648 HCAPLUS
TI Splicing method and composite circuit substrate of circuit substrate. [Machine Translation].
IN Tada, Kazuhiro; Hatanaka, Yasumichi; Fujioka, Hirofumi; Tomita, Yukihiro; Ueda, Naoto
PA Mitsubishi Electric Corp., Japan
SO Jpn. Kokai Tokkyo Koho, 17 pp.
CODEN: JKXXAF
DT Patent
LA Japanese
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001053112	A2	20010223	JP 1999-230384	19990817

AB [Machine Translation of Descriptors]. The void which remains in the **resin** composition layer is decreased, furthermore the temperature stress with the **resin** composition layer and decreases also the semiconductor **chip** and the baseplate and the splicing method of the **circuit** substrate whose reliability is high and the composite **circuit** substrate which connects the **circuit** substrate is offered. As 1st 1st the formation it does **resin** composition layer 31 on the **wiring** aspect of **circuit** substrate, 1 1st on **resin** composition layer 31 or the formation it does the 2nd **resin** composition layer 32 whose, 2nd 1st melt viscosity is lower than the **resin** composition layer on the **wiring** aspect of **circuit** substrate 5 **bump** **electrode** lying between 2 and 6, opposes arranges the **wiring** surface of the 1st and 2nd **circuit** substrate, the bonding does between the 1st and 2nd **circuit** substrate with the aforementioned **resin** composition, during aforementioned **circuit** substrate mutual **wiring connect** **electrically** with the aforementioned **bump** **electrode** .

L19 ANSWER 5 OF 6 HCAPLUS COPYRIGHT 2002 ACS

AN 1996:82901 HCAPLUS

DN 124:191386

TI **Wiring** board for semiconductor devices and its manufacture

IN Sugawa, Toshio; Kuramasu, Keizaburo

PA Matsushita Electric Ind Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 5 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 07283268	A2	19951027	JP 1994-65785	19940404

AB The title manuf. involves the following steps: (1) forming a multilayered electrode on a **wiring** board, (2) forming a fine-particle-contg. plated layer by soaking the **wiring** board in a fine-particle-contg. plating soln., (3) **elec. connecting** the plated layer and a bump on a semiconductor **chip**, and (4) attaching the **wiring** board to the semiconductor **chip** with **resin** adhesive. The **wiring** board is also claimed. Since the fine particles jut out into the bump, the plated layer on the **electrode** and the **bump** on the semiconductor **chip** are attached firmly to each other.

L19 ANSWER 6 OF 6 HCAPLUS COPYRIGHT 2002 ACS

AN 1994:122854 HCAPLUS

DN 120:122854

TI Manufacture of **wiring** board and structure of electrical connection

IN Kawamura, Yoshihiro

PA Casio Computer Co Ltd, Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

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PI JP 05167233 A2 19930702 JP 1991-361561 19911212
AB The title manuf. comprises the steps of forming a UV-blocking conductor pattern on a UV-transparent **resin** insulating substrate, forming a UV-hardenable insulating film on the overall surface, irradiating with UV light through the substrate to effect imagewise hardening of the UV-hardenable insulating film, developing to remove the UV-hardenable insulating film on the conductor pattern, and forming an opening in the hardened insulating film. The structure of **elec.** **connection** comprises an **IC chip** having the **wiring board** and a solder **bump** on an **electrode**, in which the solder bump is **elec. connected** to the conductor layer in the opening of the **wiring board**.

L24 ANSWER 1 OF 15 INSPEC COPYRIGHT 2002 IEE
AN 2001:6967500 INSPEC DN B2001-08-0170J-012
TI **Chip**-scale packaging of power devices and its application in integrated power electronics modules.
AU Xingsheng Liu (Dept. of Mater. Sci. & Eng., Virginia Polytech. Inst. & State Univ., Blacksburg, VA, USA); Xiukuan Jing; Guo-Quan Lu
SO IEEE Transactions on Advanced Packaging (May 2001) vol.24, no.2, p.206-15. 27 refs.
Doc. No.: S1521-3323(01)04492-6
Published by: IEEE
Price: CCCC 1521-3323/2001/\$10.00
CODEN: ITAPFZ ISSN: 1521-3323
SICI: 1521-3323(200105)24:2L:206:CSPP;1-N
DT Journal
TC Application; Practical; Experimental
CY United States
LA English
AB A power electronics packaging technology utilizing **chip**-scale packaged (CSP) power devices to build three-dimensional (3-D) integrated power electronics modules (IPEMs) is presented in this paper. The **chip**-scale packaging structure, termed **die** dimensional ball grid array (D2BGA), eliminates **wire** bonds by using **stacked solder joints** to interconnect power **chips**. D2BGA package consists of a power **chip**, inner solder caps, high-lead **solder balls**, and molding **resin**. It has the same lateral dimensions as the starting power **chip**, which makes high-density packaging and module miniaturization possible. This package enables the power **chip** to **combine** excellent thermal transfer, high current handling capability, improved electrical characteristics, and ultralow profile packaging. Electrical tests show that the VCE(sat) and on-resistance of the D2BGA high speed insulated-gate-bipolar transistors (IGBTs) are improved by 20% and 30% respectively by eliminating the device wirebonds and other external interconnections, such as the leadframe. In this paper, we present the design, reliability, and processing issues of D2BGA package, and the implementation of these **chip**-scale packaged power devices in building 30 kW half-bridge power converter modules. The electrical and reliability test results of the packaged devices and the power modules are reported.

L24 ANSWER 2 OF 15 INSPEC COPYRIGHT 2002 IEE
AN 2001:6858059 INSPEC DN B2001-04-0170J-024
TI **Stud bump** process of build up PWB.
AU Kato, T. (IBM Japan Ltd., Japan)
SO Proceedings. Electronic Circuits World Convention 8 Birmingham, UK: Electronics Circuits World Convention 8, 1999. p.H4ba-b, H4bh of CD-ROM pp. 3 refs.
Conference: Tokyo, Japan, 7-10 Sept 1999
Sponsor(s): Japan Printed Circuit Assoc.; Eur. Inst. of Printed Circuits; Assoc. Connecting Electron. Ind
DT Conference Article
TC Practical; Experimental
CY United Kingdom
LA English
AB Requirements for high density packaging and **wiring** have changed the structure of PWBs to playing the role of a **chip** carrier with bare **chip** attachment, which needs sophisticated **wiring** fan-out capability from the center of the bare **chip**. To meet

these requirements, SLC (surface laminar circuitTM) structure has been improved to add several features, e.g. via size reduction (mini via), copper filled via, **resin** filled PTH, etc, but the manufacturing process needs further variation to help make structures such as **stacked** vias easier. To reinforce and extend SLC manufacturing capability, a new method to make **stud bump** vias is proposed. New stud vias are carved from a plane copper foil by controlled etching called "etch down", in which etchant flow is highly controlled to secure etch uniformity on large size (500*600 mm) PWBs. Via structures with this method offer: (1) flat via surface for **joint-on-via** of matrix type flip **chip**; (2) up to 50 μ m diameter of miniaturized stackable vias to help the **chip** pads escape outward; (3) possibility of selecting nonphotosensitive insulators for material requirements such as high Tg, low CTE, low dielectric constant, etc. Another feature of this method is that the structure is realized by a combination of conventional PWB processes, which is key to minimizing process cost, though some process refinements are necessary, e.g. controlled etching. PWB requirements are clarified by formulating the fan-out capability, classifying the solutions to the requirements, and a new **stud bump** process is proposed as one of these solutions.

L24 ANSWER 3 OF 15 INSPEC COPYRIGHT 2002 IEE
 AN 1995:5074901 INSPEC DN B9511-2570-037
 TI **Chip** scale package: "a lightly dressed LSI **chip**".
 AU Yasunaga, M.; Baba, S.; Matsuo, M.; Matsushima, H. (IC Assembly Eng. Dept., Mitsubishi Electr. Corp., Hyogo, Japan); Nakao, S.; Tachikawa, T.
 SO IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A (Sept. 1995) vol.18, no.3, p.451-7. 14 refs.
 Price: CCCC 1070-9886/95/\$04.00
 CODEN: IMTAEZ ISSN: 1070-9886
 DT Journal
 TC New Development; Practical
 CY United States
 LA English
 AB A new flip-**chip**-like package named **chip** scale package (CSP) has been developed. It is constructed of LSI **chips**, thin **resin** coats, and **electrode balls**, having no leadframe nor any bonding **wires**. **Wiring** conductor patterns were used for electrical **connection** between internal pads on the **die** and external **electrode balls**. Also the transfer-bumping technique was applied for inner bump formation. Finally, solder **joint** life when **mounted** onto typical boards was estimated by simulation.

L24 ANSWER 4 OF 15 INSPEC COPYRIGHT 2002 IEE
 AN 1988:3097122 INSPEC DN B88019533
 TI MIL-P-5511 testing of microcracked kevlar printed **wiring** boards.
 AU Amick, P.J.; Cook, P.A. (McDonnell Douglas Electron. Co., St. Charles, MO, USA)
 SO Proceedings of the Technical Program of the National Electronic Packaging and Production Conference - NEPCON West '87
 Des Plaines, IL, USA: Cahners Exposition Group, 1987. p.661-7 vol.2 of 2 vol. 1050 pp. 2 refs.
 Conference: Anaheim, CA, USA, 24-26 Feb 1987
 DT Conference Article
 TC Practical
 CY United States
 LA English

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Serial No.:09/852,847

AB McDonnell Douglas Electronics Company has been actively involved for the past several years in Surface Mount Technology. In 1983, a research and development program was initiated to find a compatible printed wiring board (PWB) substrate for leadless ceramic chip carrier (LCC) mounting. Several types of resin-impregnated Kevlar systems were tested, along with other systems (including copper-Invar-copper, compliant layer, and polyimide/quartz). The most successful system passed over 1000 thermal cycles with LCCs ranging from 20 to 84 connections and consisted of Kevlar impregnated with an epoxy/polyimide blend resin (7293). During thermal cycle testing, minute cracks appeared on the surfaces of the Kevlar assemblies and were particularly noticeable near the solder pads of the LCC footprints. Cross sectioning after thermal cycling revealed that the microcracks were also throughout the Kevlar substrates, apparently propagating between the fiber bundle crossovers. There was concern as to whether or not the microcracking would become a reliability problem by serving as a path for electromigration. Electromigration occurs when voltage is applied to microcracked laminate dielectric causing leakage currents between conductors due to entrapped moisture. To test the reliability of the Kevlar substrates, several sets of PWBs were subjected to MIL-P-55110 testing.

L24 ANSWER 5 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:238545 HCAPLUS

TI Production method of semiconductor device and semiconductor device, production method of stacked type semiconductor device and stacked type semiconductor device. [Machine Translation].

IN Ouchi, Nobuhito; Shiraishi, Yasushi; Tanaka, Yasuo

PA Oki Electric Industry Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 15 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
	JP 2002093944	A2	20020329	JP 2000-274813	20000911

AB [Machine Translation of Descriptors]. The semiconductor device and its production method etc. being possible to load together the semiconductor device where function differs without making the area of the semiconductor device increase, are offered. Portion of wiring 104 is formed by also the side of semiconductor device 101, at the same time, as for projection electrode 102, in order wiring to be on 104 where that side was formed to the side of semiconductor device 101 and the abbreviation identical surface, as it is formed, ball electrode 103 at least as for part, in order to connect with wiring 104 of the semiconductor device side electrically, we are formed, and, the semiconductor device side, making wiring expose 104, as the resin it is sealed, the opposition aspect of the circuit formation aspect is sealed the resin.

L24 ANSWER 6 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:103507 HCAPLUS

DN 136:143935

TI Method of forming a stacked-die integrated circuit chip package on a wafer level

IN Lam, Ken M.

PA Atmel Corporation, USA

04/10/2002

Serial No.:09/852,847

SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6344401	B1	20020205	US 2000-521299	20000309

AB A **wafer** level packaging method which produces a **stacked** dual/multiple **die integrated circuit** package. In the method, the **wafer** with the smaller sized **dice** of two **wafers** is processed through a metal redistribution process and then **solder balls** are attached. The **wafer** is then sawed into individual **die** size ball-grid array packages. On the **wafer** with the larger sized **dice**, a **die** attached adhesive material is deposited on the front of each **die** site location that is intended for the attachment of one of the **die**-sized BGA packages. The back side of the BGA **die** package is placed onto the adhesive material and is cured. A **wire**-bonding operation connects the signals from the **die**-size BGA package to the **circuits** of the bottom **die**. A coating material, such as epoxy, is disposed on the **wafer** to cover the **wire**-bond leads and the assembly is then cured. Then, the **stacked-die wafer** is singulated into individual **stacked-die** IC packages.

RE.CNT 13 THERE ARE 13 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 7 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2002:28272 HCAPLUS

TI **Mounted** structure of semiconductor device, the packaging method and repair method. [Machine Translation].

IN Hori, Ei-ji

PA Nec Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 7 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2002009209	A2	20020111	JP 2000-190516	20000626

AB [Machine Translation of Descriptors]. This invention, **mounted** structure of the semiconductor device which makes that remove from the printed **circuit** board the semiconductor device where the seal **resin** fills up, without damaging the electrode of the printed **circuit** board or the semiconductor device, possible, designates the offer of the packaging method and repair method as purpose. When semiconductor device true form 1 and printed **circuit** board 2 and semiconductor device true form the **solder ball** 3 which connects 1 and printed **circuit** board 2 electrically and semiconductor device true form fills up with 1 and printed **circuit** board and 2 semiconductor device true form distribution facilities it is done with 1 and printed **circuit** board 2 these the bonding the seal **resin** 5 which is done and, in the **mounted** structure of the semiconductor device which consists of, is moved mandatorily is made the constitution which the **wire** 4 which makes crack seal **resin** cause 5, consists of the insulated

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ingredient ingredient preparation is done.

L24 ANSWER 8 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:847816 HCAPLUS

DN 135:379675

TI Method and sheet for **mounting** semiconductor **chip** on printed **wiring** board

IN Nishihara, Kunio

PA Mitsui Chemicals Inc., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001326246	A2	20011122	JP 2000-139662	20000512
AB	The title method involves prepg. a chip-mounting sheet of a synthetic resin film having a thermosetting resin layer whose thickness is similar to that of the height of a bump electrode of the chip , pressing the thermosetting resin layer to the bump side of the chip , peeling off the synthetic resin film, positioning the chip to align the bump electrode to the electrode of the wiring board, and joining the electrodes together as well as hardening the thermosetting resin . Specifically, the thermosetting resin may comprise an epoxy resin .				

L24 ANSWER 9 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:762682 HCAPLUS

TI Semiconductor device and its production method. [Machine Translation].

IN Fujimoto, Hiroaki; Nomura, Toru

PA Matsushita Electric Industrial Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 8 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001291821	A2	20011019	JP 2000-106035	20000407
AB	[Machine Translation of Descriptors]. In case of 1 tip/ chip structure, correspondence to the semiconductor equipment component which future diversifies and decrease of number of articles with the loading device not be able to correspond to the multi-function semiconductor device to the miniaturization and light weight conversion of the electronic equipment with that cannot correspond. Vis-a-vis insulated baseplate 8 by 2nd semiconductor component possesses with the 1st laminated body which is 12 and 3rd semiconductor component 13 and furthermore by 4th semiconductor component the 2nd laminated body which is 14 and 5th semiconductor component 15 in the 1st semiconductor component 10 which is connected by bump electrode 9 and the top, the 1st laminated body, the 2nd laminated body and the electrode of insulated baseplate 8 appearance are connected with each metal thin line, to be a semiconductor device where outside enclosure of appearance of insulated baseplate 8 is sealed with seal resin 20, the laminated body Multifunctions and high density can be actualized the laminate with the structure which is mounted with each three dimensions.				

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L24 ANSWER 10 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:611707 HCAPLUS

DN 135:161252

TI Inexpensive and reliable BGA package for high density cavity-up
wire bond device **connections** using a metal panel, thin
film and build up multilayer technology

IN Ho, Chung Wen

PA Thin Film Module, Inc., Taiwan

SO U.S., 11 pp.

CODEN: USXXAM

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6277672	B1	20010821	US 1999-389634	19990903
	US 2001046725	A1	20011129	US 2001-900558	20010709
PRAI	US 1999-389634	XX	19990903		

AB A new method is provided for **mounting** high-d. **wire**
bond semiconductor devices. A layer of dielec. is deposited over the 1st
surface of a metal panel. One or more thin film interconnect layers are
then created on top of the dielec. layer. The BUM technol. allows for the
creation of a succession of layers over the thin film layers. The
combined layers of thin film and BUM form the interconnect substrate. One
or more cavities are created in the 2nd surface of the metal panel;
openings through the layer of dielec. are created where the layer of
dielec. is exposed. One or more **wire** bond semiconductor
die are inserted into the cavities, are **die** bonded and
wire bonded to the openings that were created in the layer of
dielec. Openings are created in the bottom BUM layer; **solder**
balls are inserted and attached to this BUM layer for the
completion of the Ball Grid Array (BGA) package.

RE.CNT 11 THERE ARE 11 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 11 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:507236 HCAPLUS

DN 135:203631

TI **Chip**-scale packaging of power devices and its application in
integrated power electronics modules

AU Liu, Xingsheng; Jing, Xiukuan; Lu, Guo-Quan

CS Power Electronics Packaging Laboratory, Materials Science and Engineering
Department, Center for Power Electronics Systems, Virginia Polytechnic
Institute and State University, Blacksburg, VA, 24061, USA

SO IEEE Transactions on Advanced Packaging (2001), 24(2), 206-215

CODEN: ITAPFZ; ISSN: 1521-3323

PB Institute of Electrical and Electronics Engineers

DT Journal

LA English

AB A power electronics packaging technol. using **chip**-scale packaged
(CSP) power devices to build three-dimensional (3-D) integrated power
electronics modules (IPEMs) is presented. The **chip**-scale
packaging structure, termed **die** dimensional ball grid array
(D2BGA), eliminates **wire** bonds by using **stacked** solder
joints to interconnect power **chips**. D2BGA package
consists of a power **chip**, inner solder caps, high-lead
solder balls, and molding **resin**. It has the
same lateral dimensions as the starting power **chip**, which makes

high-d. packaging and module miniaturization possible. This package enables the power **chip** to **combine** excellent thermal transfer, high current handling capability, improved elec. characteristics, and ultralow profile packaging. Elec. tests show that the VCE(sat) and on-resistance of the D2BGA high speed insulated-gate-bipolar transistors (IGBTs) are improved by 20% and 30% resp. by eliminating the device wirebonds and other external interconnections, such as the leadframe. The authors present the design, reliability, and processing issues of D2BGA package, and the implementation of these **chip**-scale packaged power devices in building 30 kW half-bridge power converter modules. The elec. and reliability test results of the packaged devices and the power modules are reported.

RE.CNT 27 THERE ARE 27 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L24 ANSWER 12 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:415430 HCAPLUS

TI Packaging method of semiconductor **chip**, and production method of electromagnetic wave reading possible data carrier. [Machine Translation].

IN Kawai, Wakahiro

PA Omron Corp., Japan

SO Jpn. Kokai Tokkyo Koho, 17 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001156110	A2	20010608	JP 1999-333409	19991124
	CN 1300180	A	20010620	CN 2000-128333	20001124
PRAI	JP 1999-333409	A	19991124		

AB [Machine Translation of Descriptors]. The semiconductor **chip** quickly, electrically and mechanically securely, furthermore the packaging method of the semiconductor **chip** due to the **mounted** possible flip tip/**chip** connected method is offered to low cost, on the **wiring** baseplate. By granting the ultrasound continuously in a state where have contacted with process and aforementioned **bump** and the **electrode** territory which **bump** of the semiconductor bear tip/**chip** while the addition doing the ultrasound, pushing away the thermoplastic **resin** coat which melted by the thing which push, make with **bump** and the **electrode** territory with respect to the thermoplastic **resin** coat which to the molten state contact is the thermoplastic **resin** coat which covers the electrode territory on the **wiring** pattern in a state where is made to heat is made to melt,, process and the description above which the ultrasound bonding can point **bump** and the **electrode** territory the cooling solidification being able to point to the thermoplastic **resin** which was melted, the process adhesion the semiconductor bear tip/**chip** true form on the **wiring** baseplate and, Ingredient preparation it does.

L24 ANSWER 13 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2001:226286 HCAPLUS

TI Semiconductor device and its production method. [Machine Translation].

IN Yamada, Munehiro; Masuda, Masachika

PA Hitachi, Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 16 pp.

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Serial No.:09/852,847

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2001085609	A2	20010330	JP 1999-263645	19990917
AB	[Machine Translation of Descriptors]. Thin-shaped conversion of the semiconductor device which 2 semiconductor chips the resin is sealed the propulsion is done. In addition, decrease of the solder connected life which originates in the thermal difference of expansion coefficient of the baseplate and the semiconductor chip of this semiconductor device is retarded. The CSP of this invention, in order for mutual back to oppose, 2 tips/ chips 1 A and 1 A laminates through elastomer & sheet 4, adheres to the appearance of based baseplate, 5 seals with mold resin 2. Elastomer & sheet 4, it consists of the ingredient whose elasticity is higher than based baseplate 5, the stress which occurs the baseplate and due to the thermal difference of expansion coefficient of tip/ chip 1 A the CSP is mounted eases, absorbs, retards the decrease of connected life of bump electrode 9. 2 tips/ chips 1 A and 1 A are connected , through wire 8 A and 8 B, all over the formation of based baseplate 5 Cu wiring 6 which is done electrically.				

L24 ANSWER 14 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 2000:747538 HCAPLUS

TI Structure and its production method of flip tip/**chip** **mounted** formula semiconductor **chip**. [Machine Translation].

IN Shimogai, Kouji

PA Rohm Co., Ltd., Japan

SO Jpn. Kokai Tokkyo Koho, 6 pp.

CODEN: JKXXAF

DT Patent

LA Japanese

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	JP 2000299409	A2	20001024	JP 1999-108776	19990416
AB	[Machine Translation of Descriptors]. With the anisotropic electric conduction film piece 3 which wears semiconductor chip 1 on the surface of particular semiconductor chip 1 vis-a-vis circuit baseplate 5, in this, the sealed function for the static electricity and noise et cetera the addition is done in the flip tip/ chip mounted formula semiconductor chip that, is connected to the wiring pattern 9 in the electrode bump 2 circuit baseplate 5 simultaneously adhesion & adheres electrically. On the peripheral aspect in aforementioned semiconductor chip 1 and the peripheral aspect in aforementioned anisotropic electric conduction film piece 3, coats the carbide of the synthetic resin in aforementioned anisotropic electric conduction film piece 3 4 the formation.				

L24 ANSWER 15 OF 15 HCAPLUS COPYRIGHT 2002 ACS

AN 1997:411109 HCAPLUS

DN 127:103020

TI Ball grid assembly type semiconductor device having a heat diffusion function and an electric and magnetic shielding function

04/10/2002

Serial No.:09/852,847

IN Nakashima, Takashi
PA Mitsui High-Tec, Inc., Japan
SO U.S., 8 pp.
CODEN: USXXAM
DT Patent
LA English
FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 5640047	A	19970617	US 1996-641351	19960430
PRAI	JP 1995-271791		19950925		

AB A semiconductor device comprises a **circuit** substrate provided with 1st and 2nd lead patterns on the front and rear surfaces, resp. The 1st lead pattern includes a **die mounting** region and conductive leads. The 2nd lead pattern includes 1st outer **connecting** terminal lands **connected** with the **die mounting** region by way of 1st vias, 2nd outer **connecting** terminal lands **connected** with the conductive leads of the 1st lead pattern by way of 2nd vias, and a ground plane **connected** with the 1st outer **connecting** terminal lands while being elec. and magnetically shielded from the 2nd outer **connecting** terminal lands. **Solder balls** are **mounted** on the 1st and 2nd outer **connecting** terminal lands. A semiconductor **die** is **mounted** on the **die mounting** region. Bonding **wires** **connect** electrode pads **mounted** on the semiconductor **die** with the conductive leads. A **resin** package seals the semiconductor **die** and the bonding **wires** on the front surface of the **circuit** substrate. The semiconductor device effectively restricts the occurrence of cross talk noise caused by parasitic current in the conductive layer, improves the heat diffusion of the semiconductor device, and effectively prevents malfunctions of semiconductor devices caused by electromagnetic noise.